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Compal Confidential

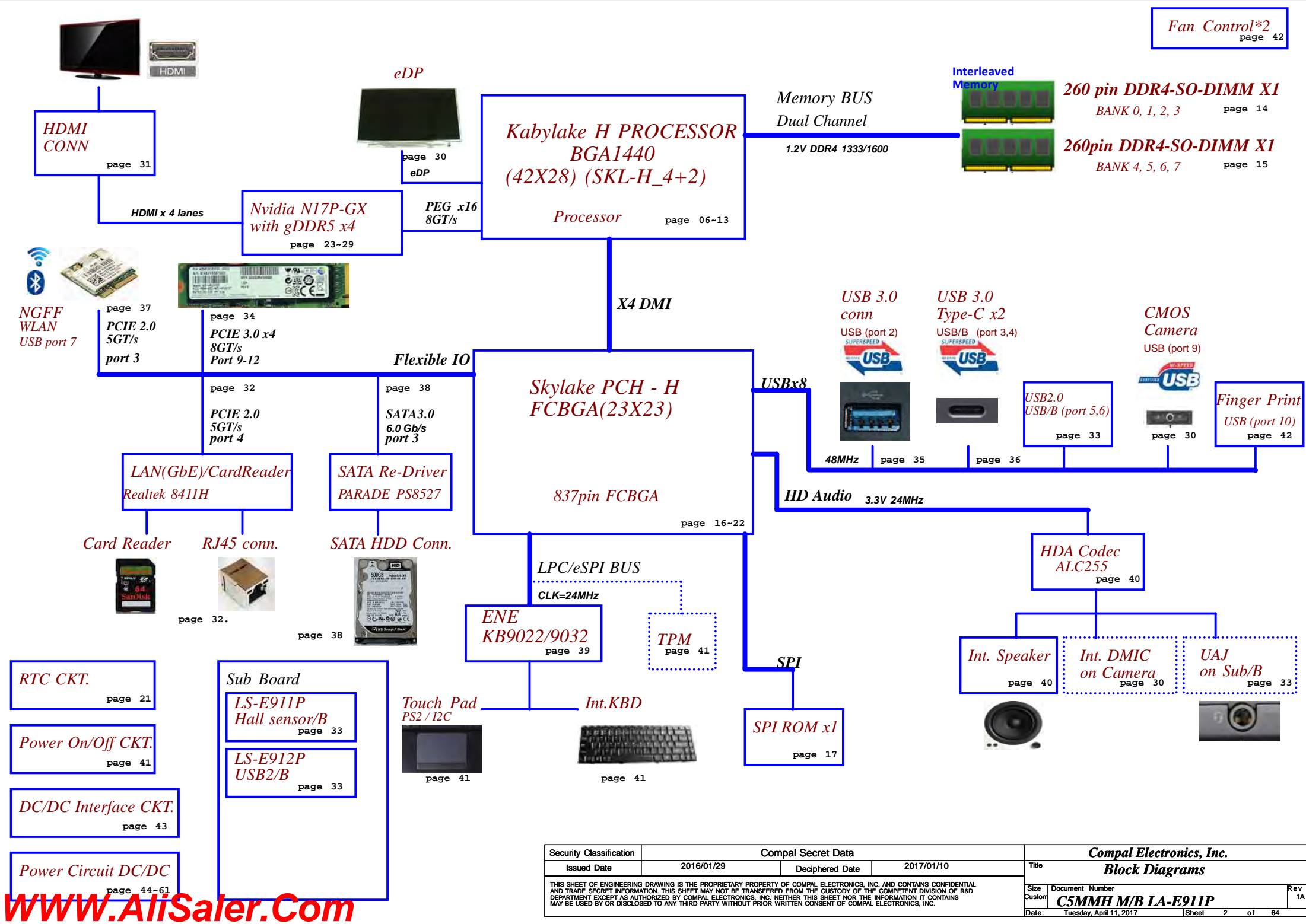
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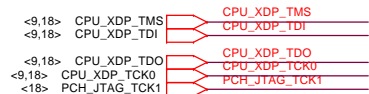
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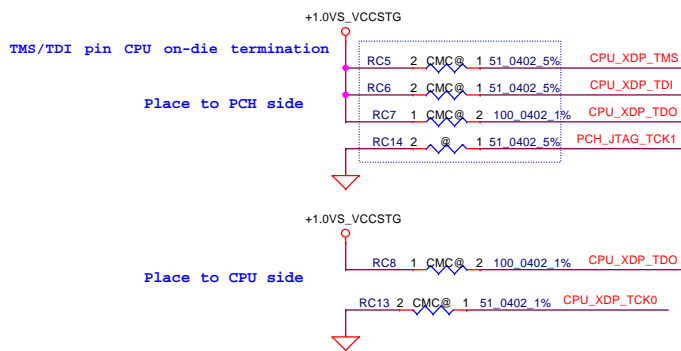
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If need debug from usb port. this cmc@ need pop



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SR32S@

UC1
SR32Q@

UH1
SR30W@

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G0@

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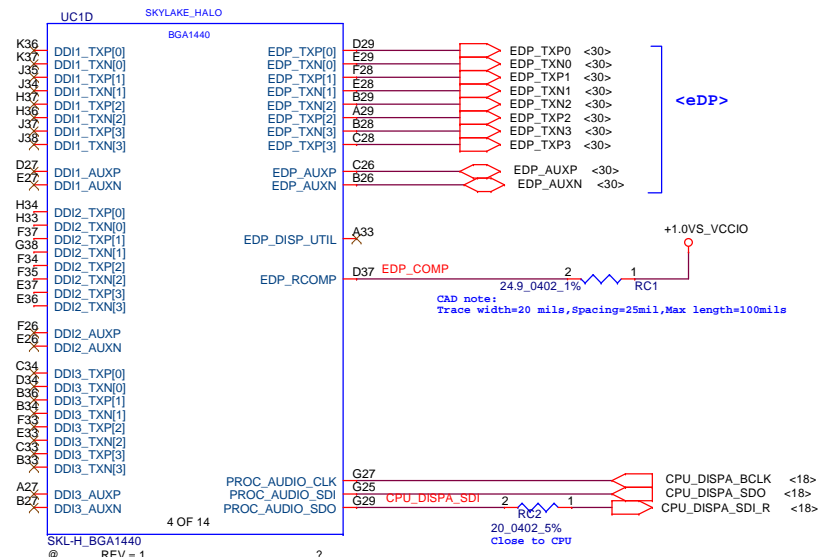
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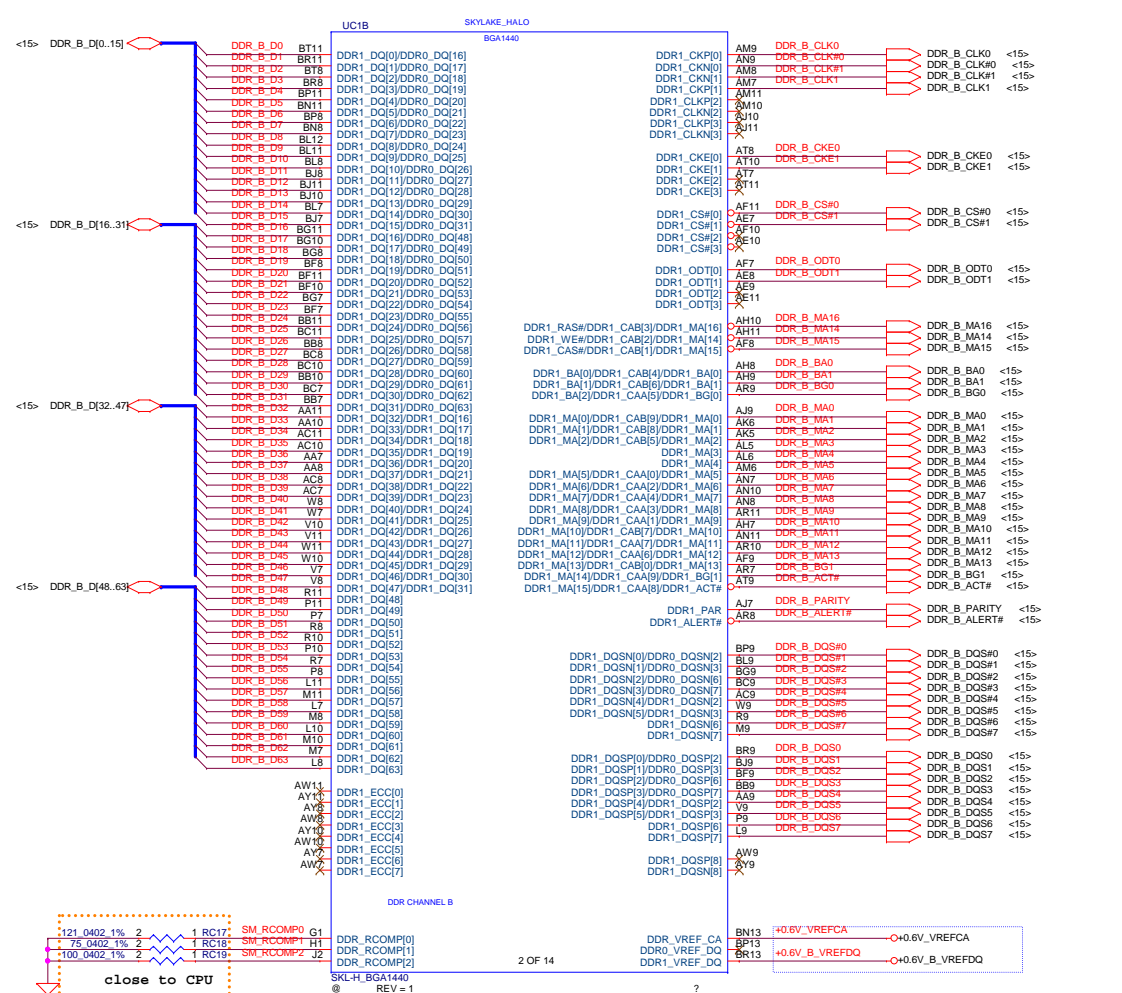
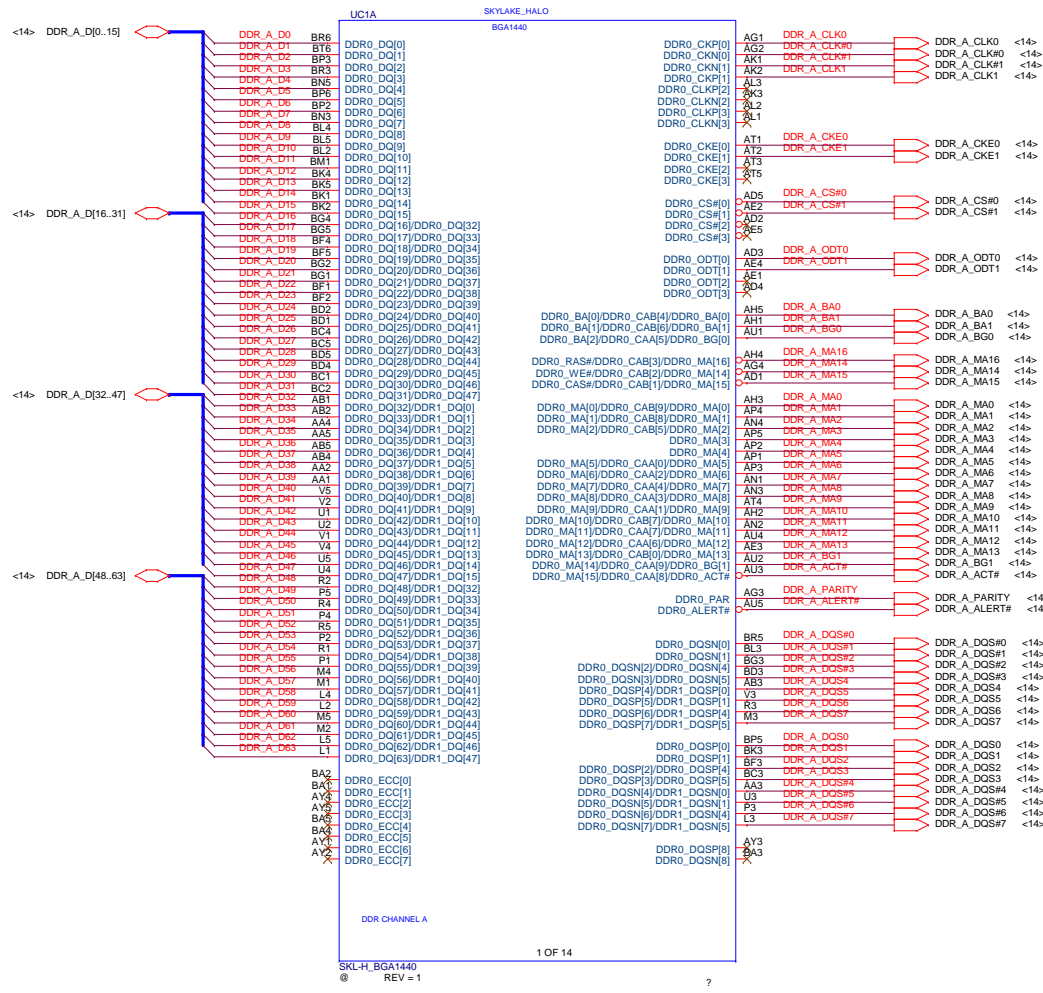
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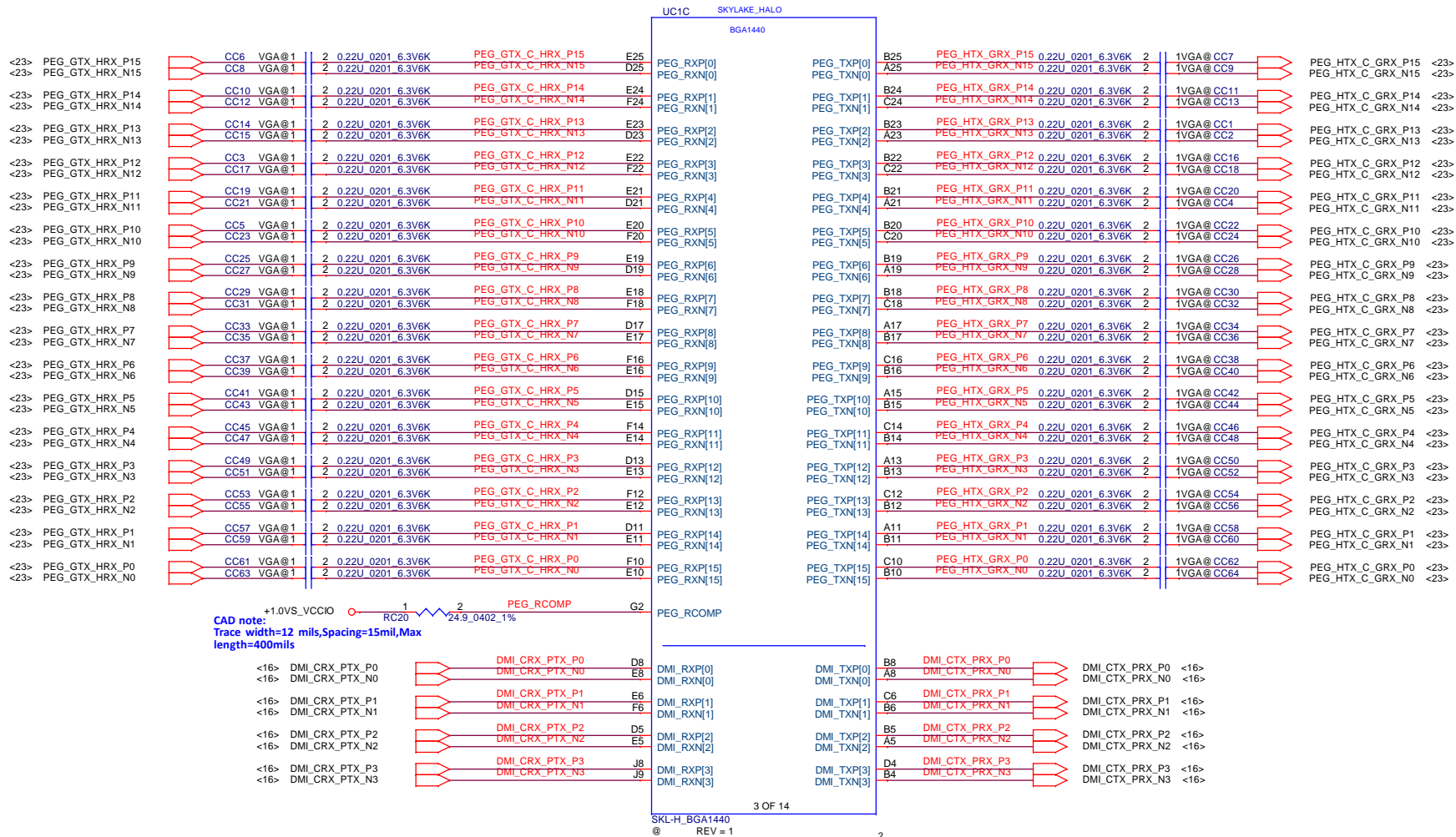
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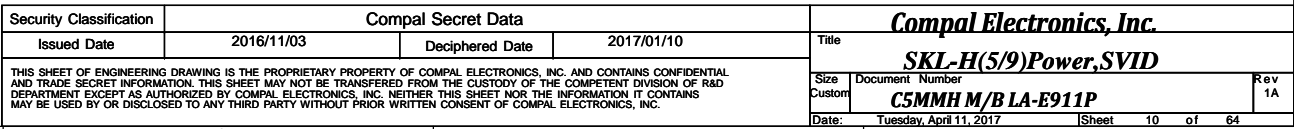


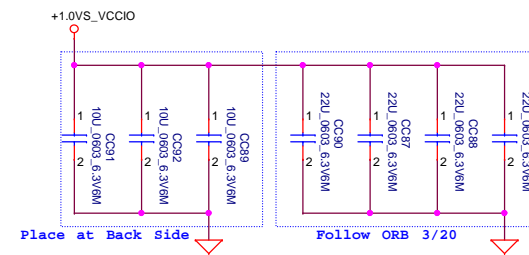
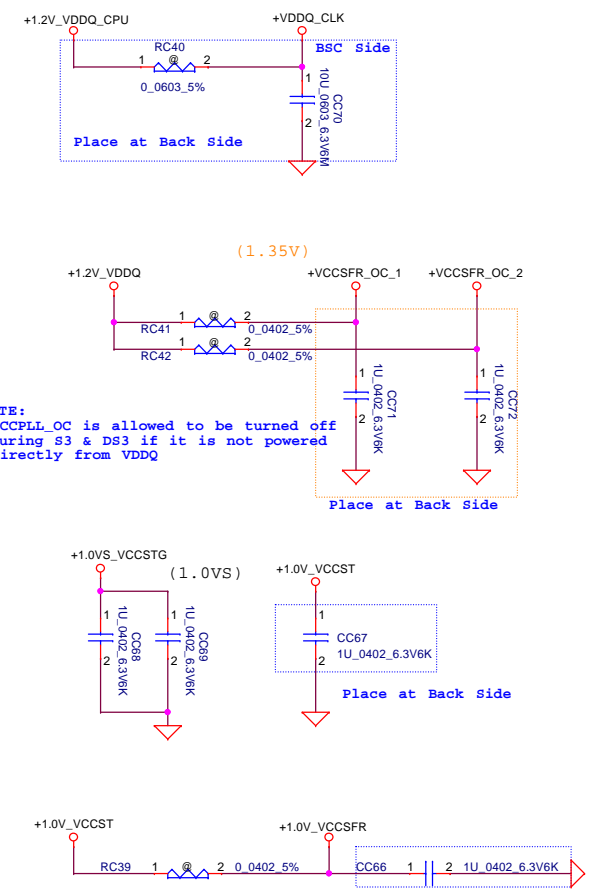
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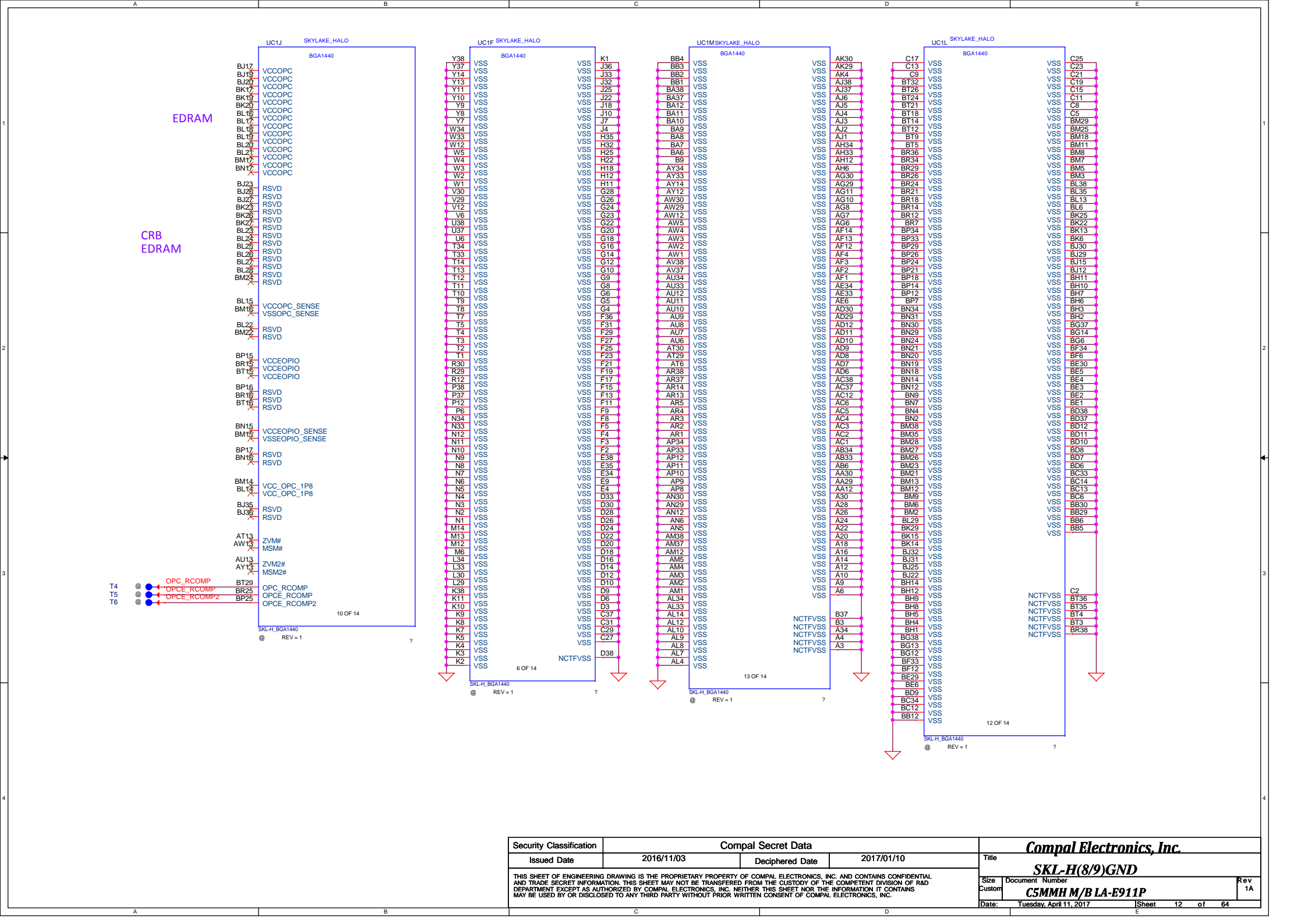
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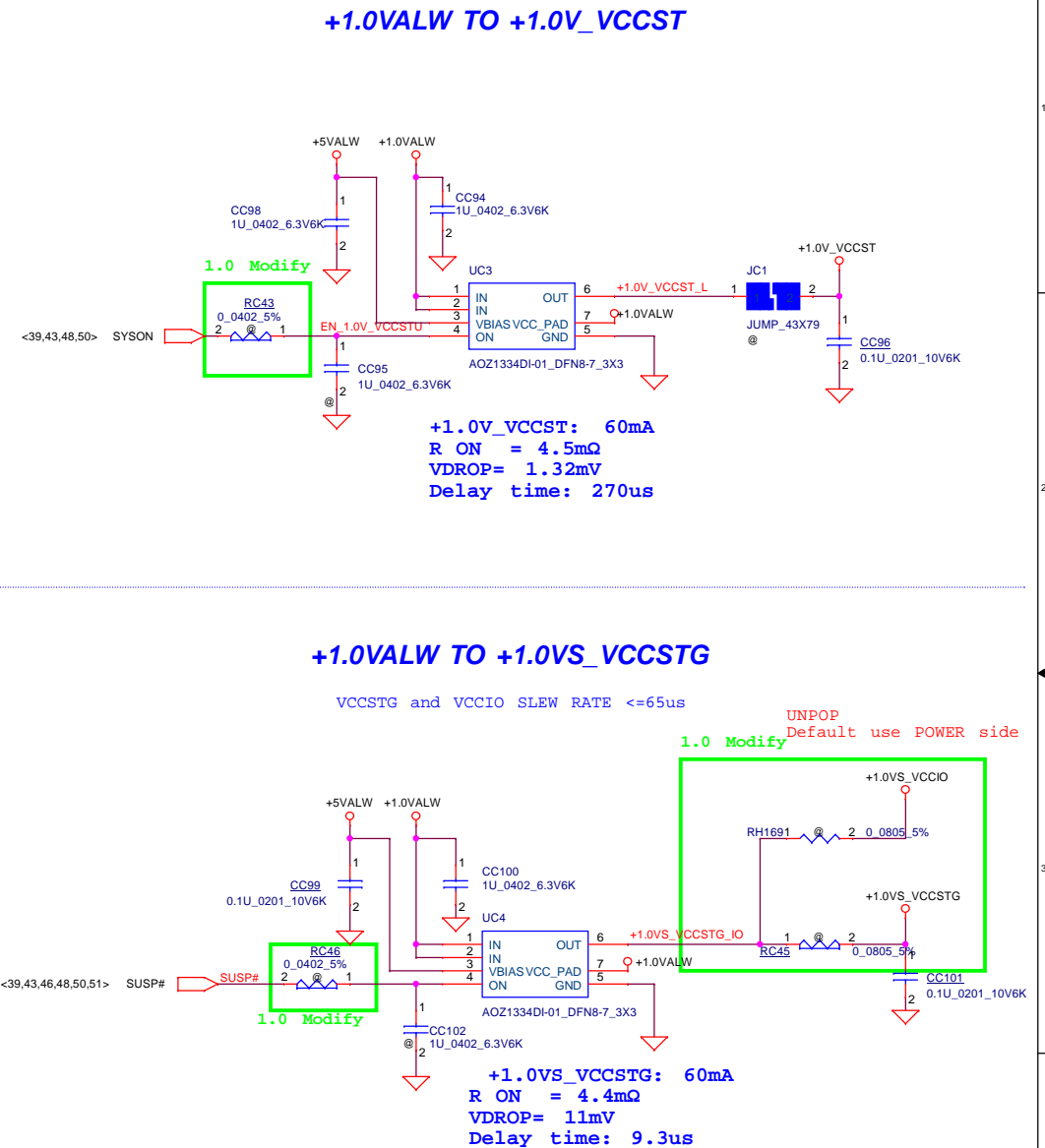




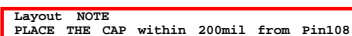
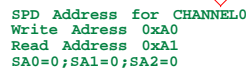
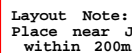
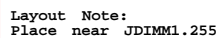
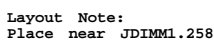
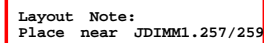
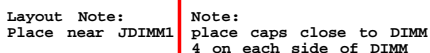


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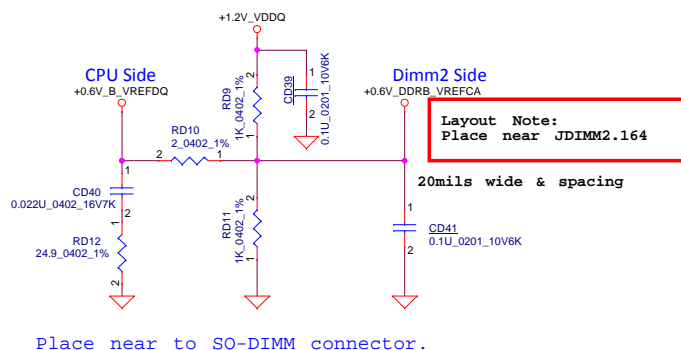


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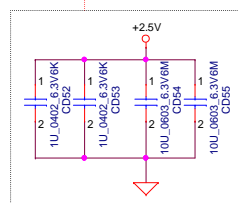
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2-3A to 1 DIMMs/channel

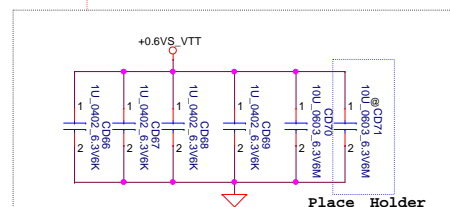


Note:
place caps close to DIMM
4 on each side of DIMM

Layout Note:
Place near JDIMM2 257/259

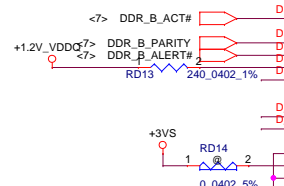


Layout Note:
Place near JDIMM2.258

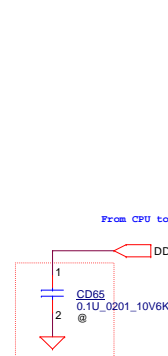


Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1.164
within 200mils

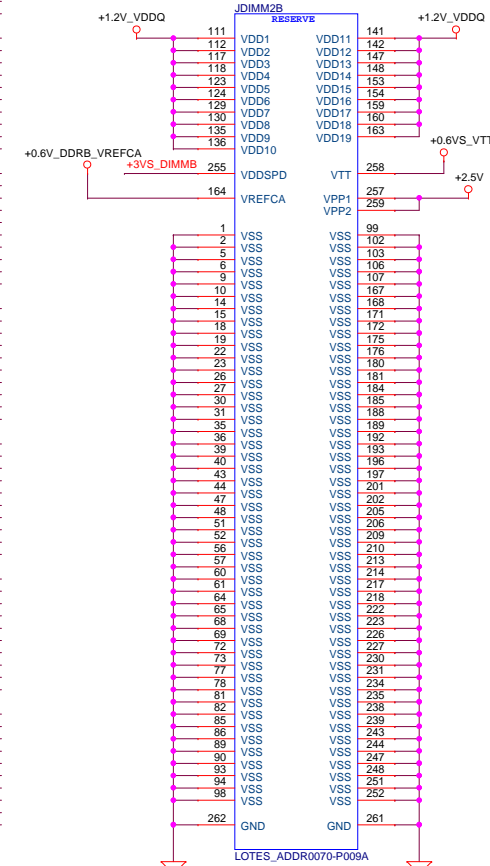


```
SPD Address for CHANNELB
Write Address 0xA4
Read Address 0xA3
SA0=0;SA1=1;SA2=0
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Layout NOTE
PLACE THE CAP within 200mil from Pin108
*2015MOW02, Can't install Cap on DRAMRST

DDR_B_CLK0	137																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
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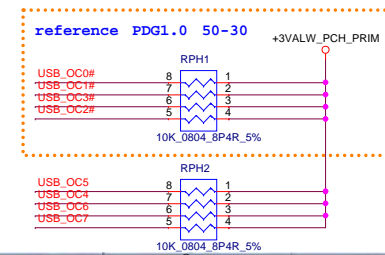
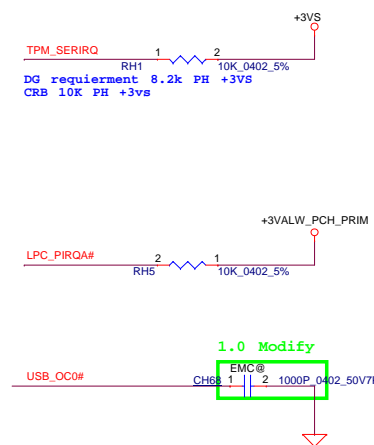
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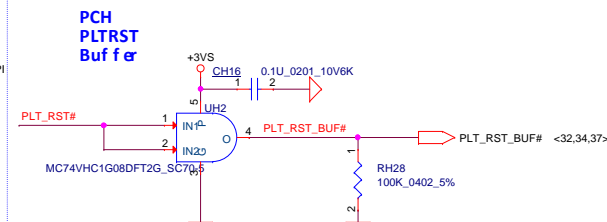
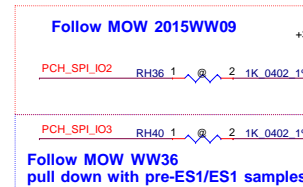
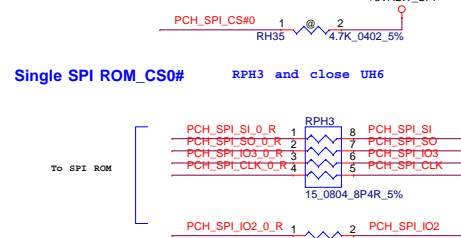
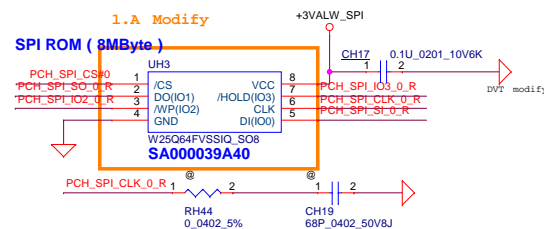
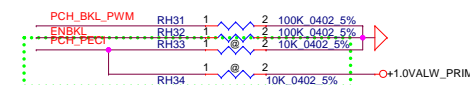
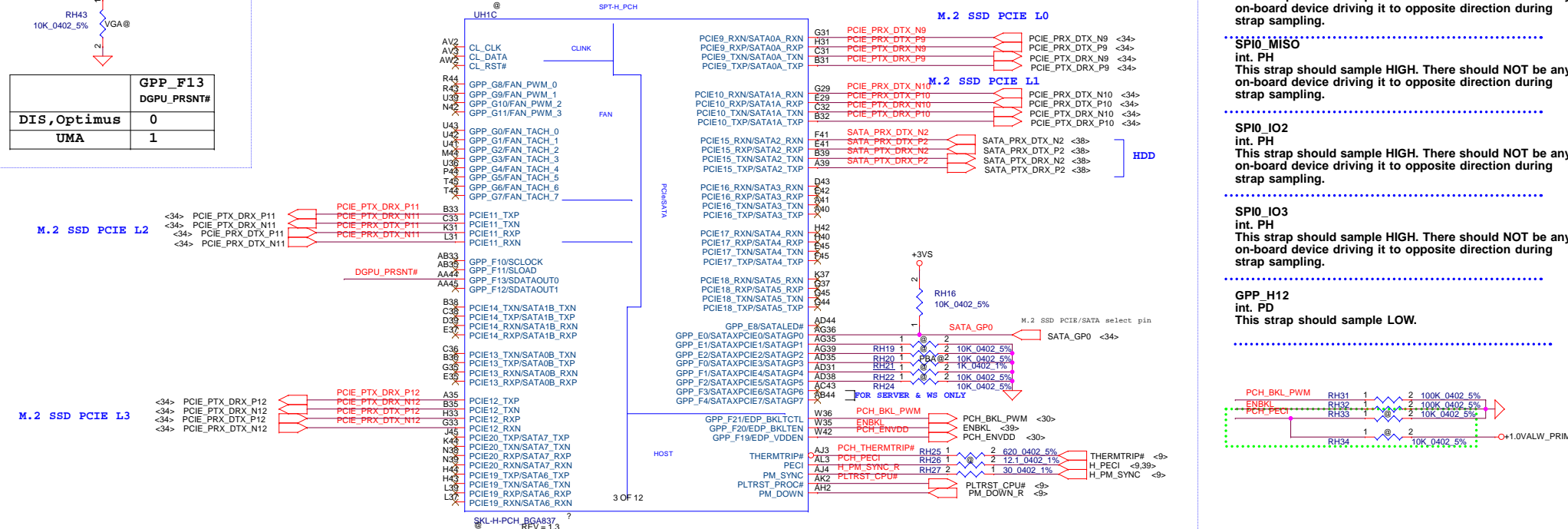
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				Custom	1A
				C5MMH M/B LA-E911P	
Date:				Tuesday, April 11, 2017	Sheet 16 of 64



	GPP_F13 DGPU_PRSNT#
DIS,Optimus	0
UMA	1



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				Custom	C5MMH M/B LA-E911P	1.
Date:				Tuesday, April 11, 2017	Sheet	17 of 64

Functional Strap Definitions

GPIO1_MOSI / GPP_B22

int. PD

Boot BIOS Destination

0 = SPI (Default)

1 = LPC

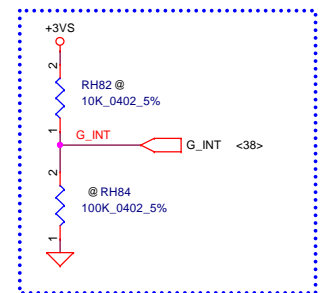
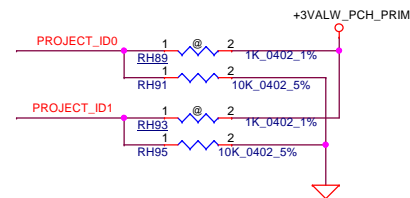
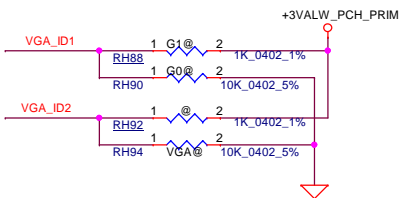
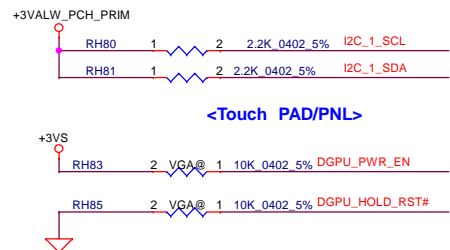
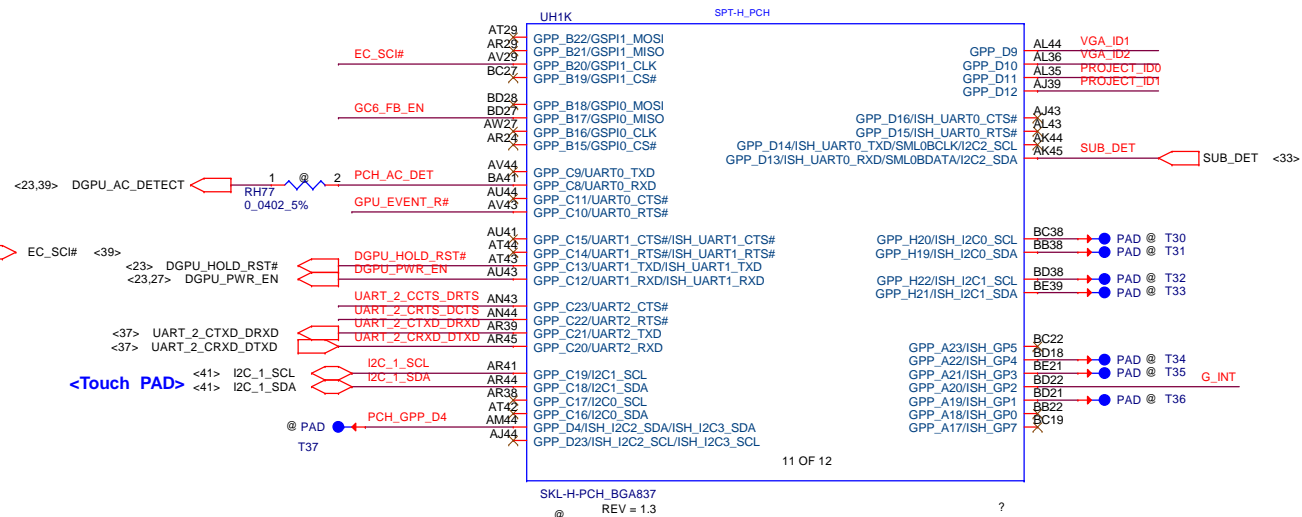
GPIO0_MOSI / GPP_B18

int. PD

0 = Disable No Reboot mode. (Default)

1 = Enable No Reboot mode (PCH will disable the TCO

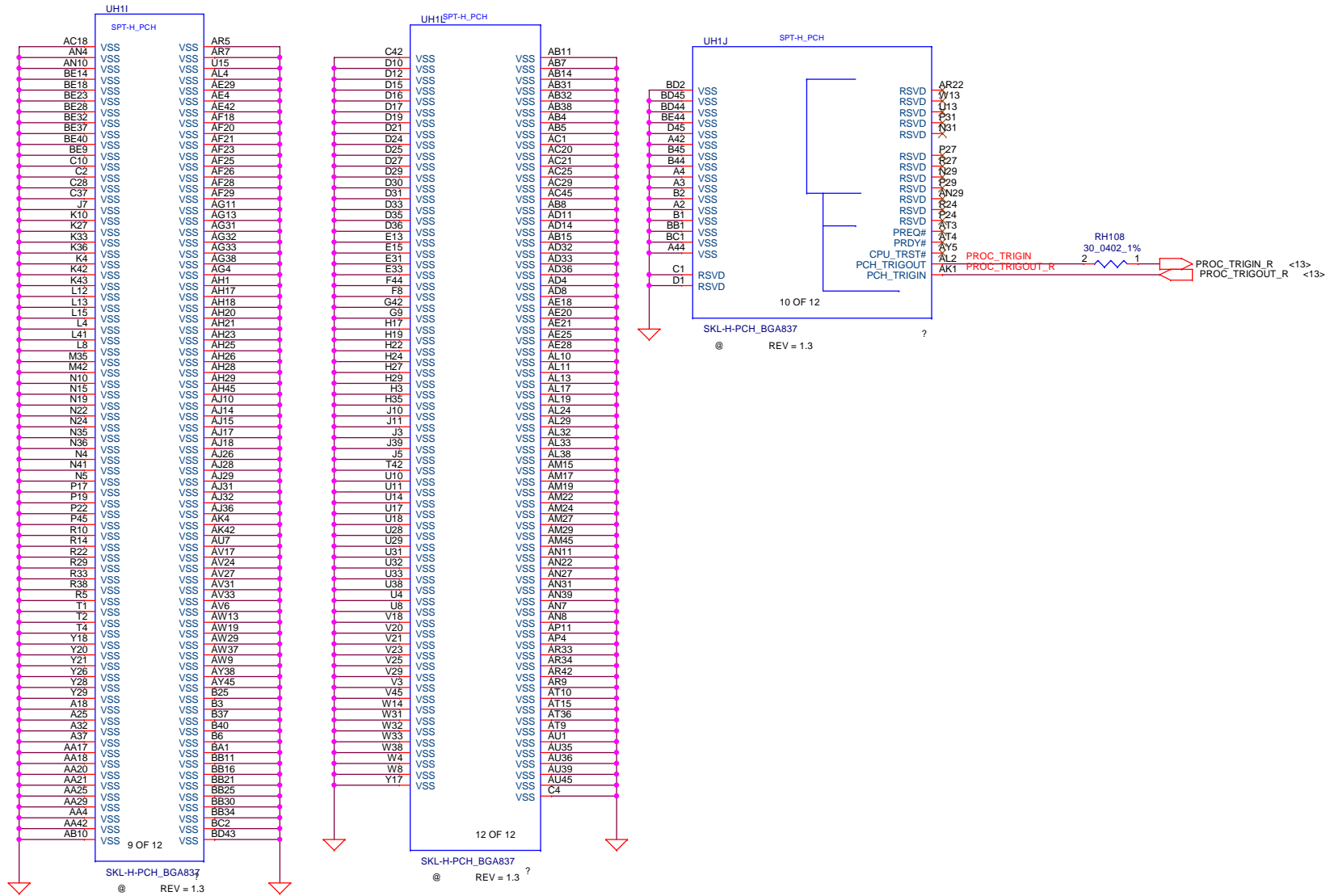
Timer system reboot feature).

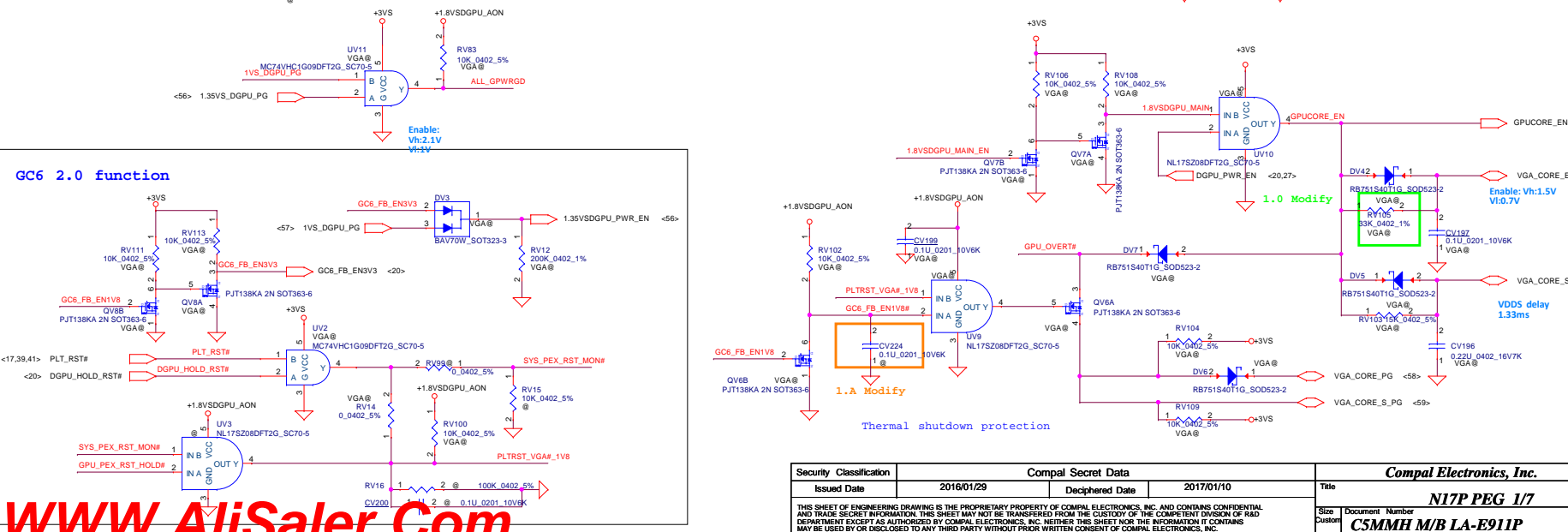


TO DGPU

VGA ID	VGA_ID2 GPP_D10	VGA_ID1 GPP_D9
N17P-G0	0	0
N17P-G1	0	1
N17E-G1	1	0
Reserved	1	1

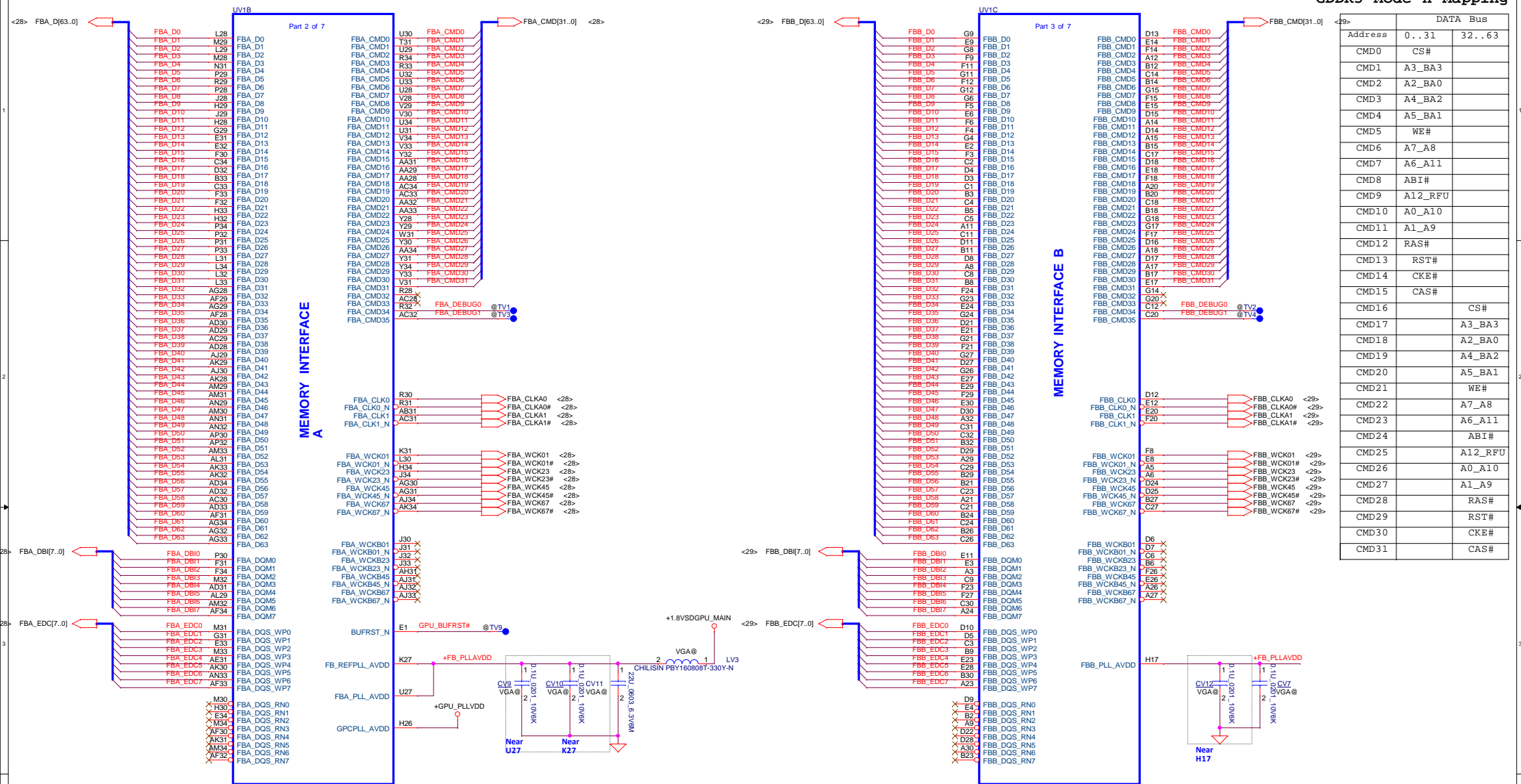
Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
*C5MMH	0	0
C5PRH	0	1
Reserved	1	0
Reserved	1	1





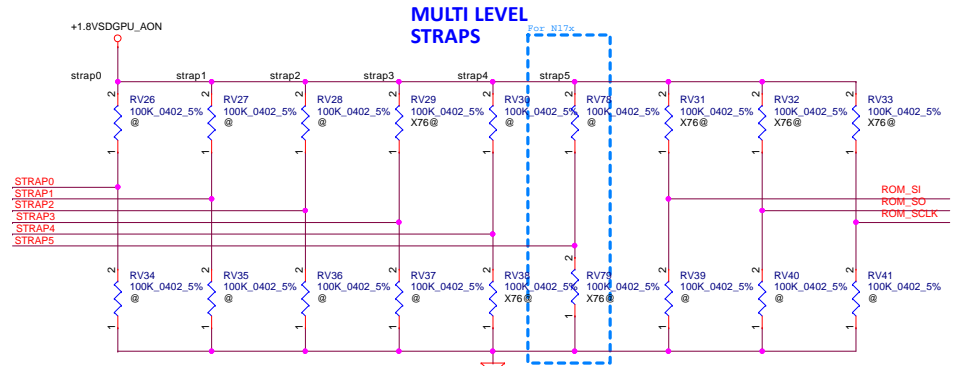
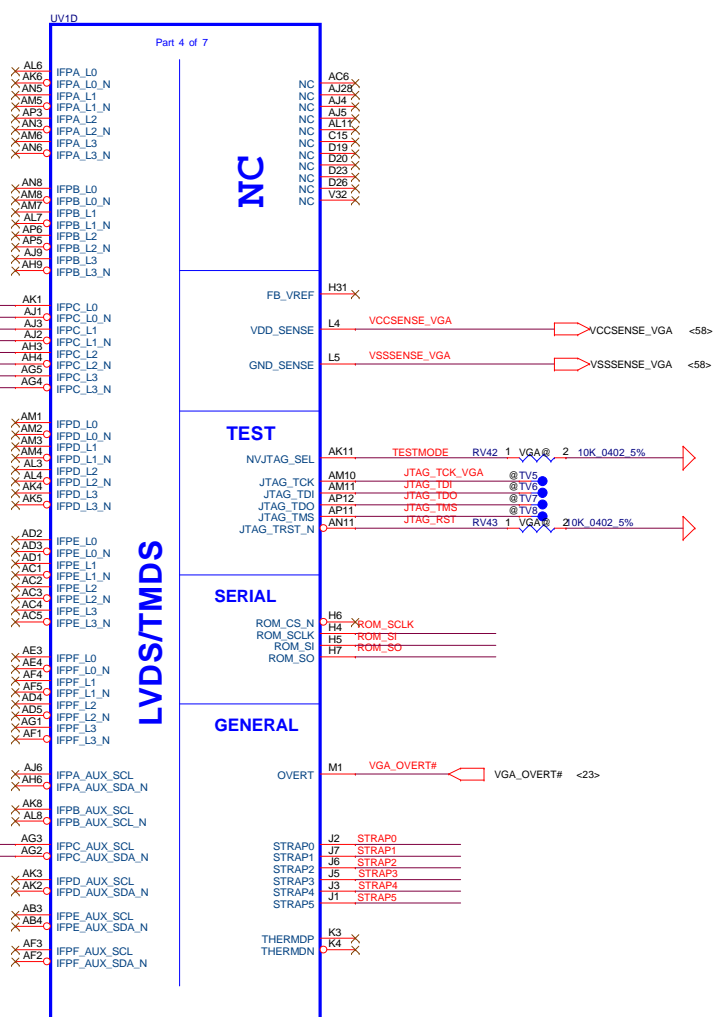
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GDDR5 Mode H Mapping



Address	DATA	Bus
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

HDMI 2.0



Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V ²	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production candidate
4 Gb	128Mx32	1.35V and 1.5V ²	Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production candidate
			Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production candidate
			Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production candidate

Table 5.2 RAMCFG

Strap Pins see Note	RAMCFG Setting Number
STRAP2 STRAP1 STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L L L	0 (0x0000)
L L H	1 (0x0001)
L H L	2 (0x0002)
L H H	3 (0x0003)
H L L	4 (0x0004)
H L H	5 (0x0005)
H H L	6 (0x0006)
H H H	7 (0x0007)
L L M	8 (0x0008)
L M L	9 (0x0009)
L M H	10 (0x000A)
L H M	11 (0x000B)
M L L	12 (0x000C)
M L H	13 (0x000D)

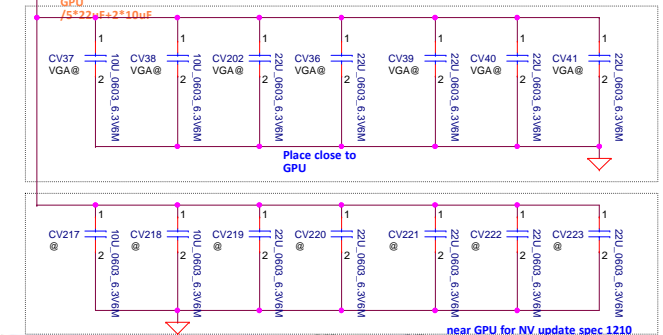
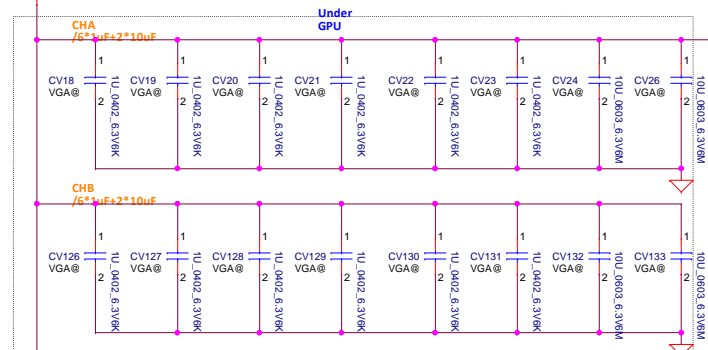
Table 5.4 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note	Resulting SORx_EXPOSED Enablements
	ROM_SO ROM_SI ROM_SCLK SOR3_EXPOSED SOR2_EXPOSED SOR1_EXPOSED SOR0_EXPOSED	
15	L L L	ENABLED ENABLED ENABLED ENABLED
14	L L H	ENABLED ENABLED ENABLED disabled
13	L H L	ENABLED ENABLED disabled ENABLED
12	L H H	ENABLED disabled disabled disabled
11	H L L	ENABLED disabled ENABLED ENABLED
10	H L H	ENABLED disabled ENABLED disabled
8	H H H	disabled disabled disabled disabled
0	H H M	disabled disabled disabled disabled
	M X X	(Reserved; do not configure)
	All other Strap Configurations	(Reserved)

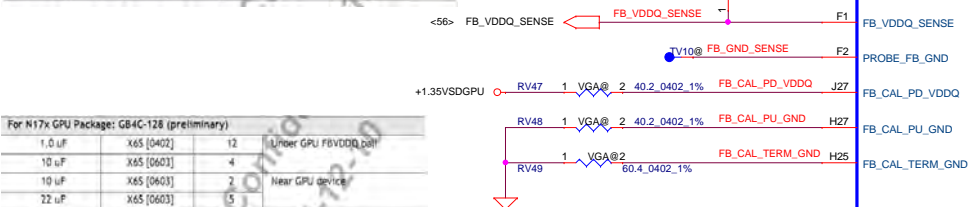
HDMI audio output

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+1.35VSDGPU



Memory	FBVDDQ	FB_CAL_PU_GND	FB_CAL_PD_VDDQ	FB_CAL_TERM_GND
GDOR5	1.5 V	40.2 Ω	40.2 Ω	60.4 Ω
GDOR5	1.55 V	40.2 Ω	40.2 Ω	60.4 Ω
GDOR5	1.35 V	40.2 Ω	40.2 Ω	60.4 Ω

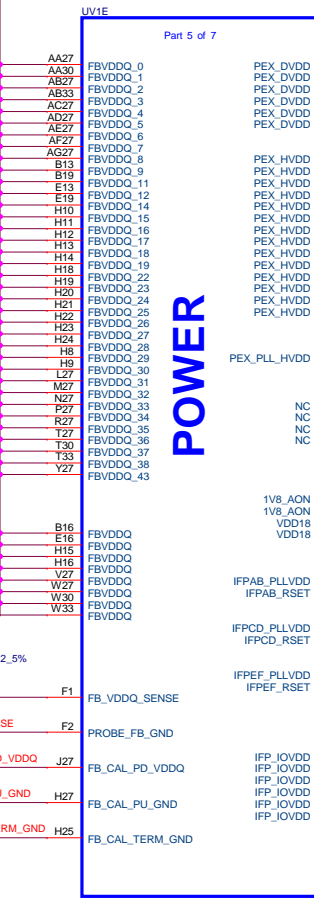


For N17x GPU Package: GB4C-128 (preliminary)				
Capacitor Type	Footprint	Population	N16	N17
1.0 uF	X65 [0402]	12	2	4
10 uF	X65 [0603]	4	2	2
10 uF	X65 [0403]	2	2	2
22 uF	X65 [0603]	5	2	1

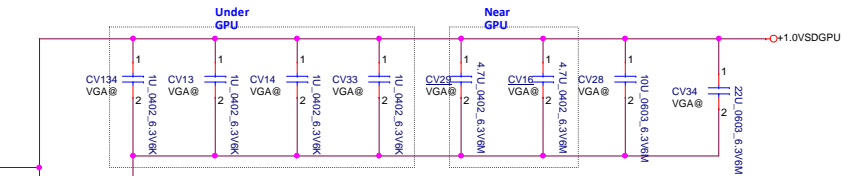
GPU	Type	Footprint	N16	N17	Location
N16P: IFP(C, D, E), PLLVDD or N16E: IFP(C, E), PLLVDD Supply Rails					
GB4B-128, GB4C-128	0.1 uF	X7R 0402	3	2	N16P: Under GPU, 1 per ball
	1.0 uF	X6S 0402	1	0	N16E: Under GPU, 1 per ball
	4.7 uF	X5R 0603	1	0	Near GPU
Bead Type					
	L2-300 Ω @ 100 MHz (ESR=0.25 Ω)	0603	1	0	Near GPU

GPU	Type	Footprint	N16	N17	Location
IFP_Y_IOVDD (N17 IFP_YIOVDD) Supply Rails					
GB4B-128, GB4C-128	0.1 uF	X7R 0402	6	6	Under GPU, 1 per ball
	1.0 uF	X6S 0402	2	3	Near GPU
	4.7 uF	X6S 0603	2	3	Near GPU
Bead Type					
	L1=180 Ω @ 100 MHz (ESR=0.2 Ω)	0603	2	0	Near GPU

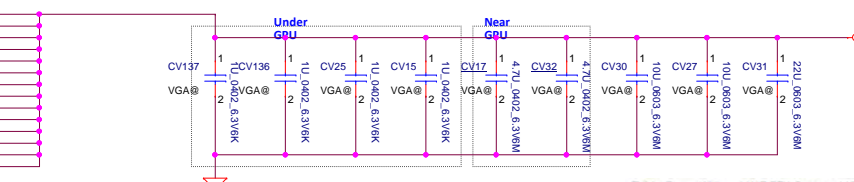
POWER



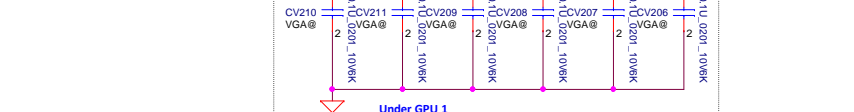
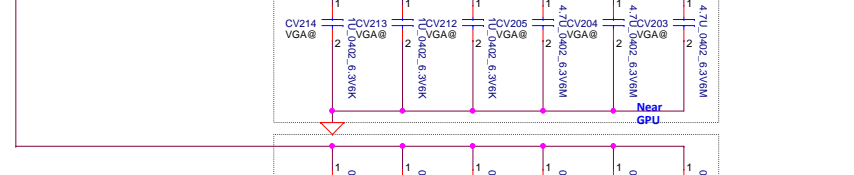
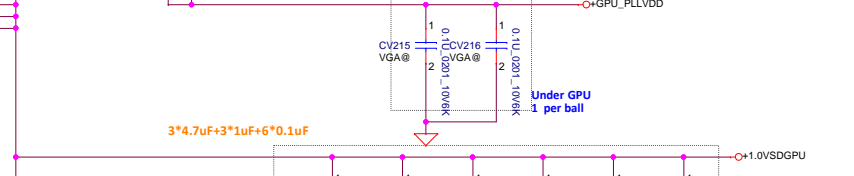
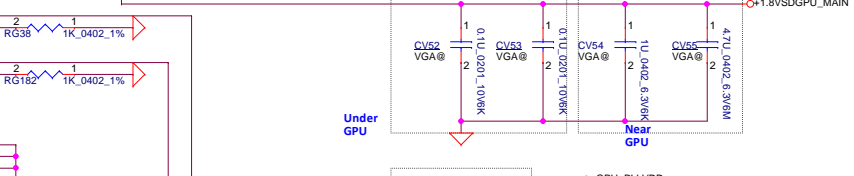
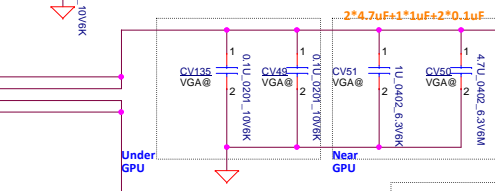
1*22uF+1*10uF+2*4.7uF+4*1uF



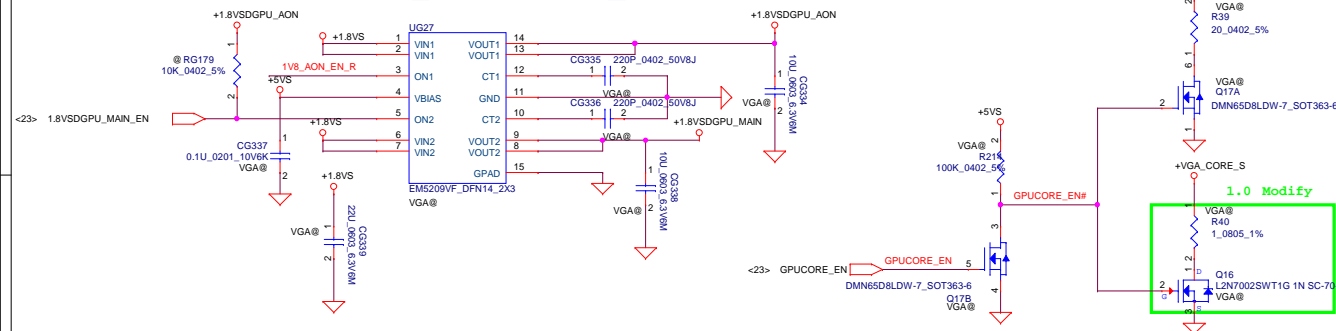
1*22uF+2*10uF+2*4.7uF+4*1uF



GPU	Capacitor Type	Footprint	Population	N16	N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB4B-128, GB4C-128	1.0 uF	X65 0402	2	4	2	Under GPU
	4.7 uF	X6S 0603	1	2	2	Near GPU
	10 uF	X5R 0805	2	1	1	Midway between GPU and Power Supply
	22 uF	X5R 0805	2	1	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB4B-128, GB4C-128	1.0 uF	X65 0402	2	4	2	Under GPU
	4.7 uF	X6S 0603	1	2	2	Near GPU
	10 uF	X5R 0805	2	2	2	Midway between GPU and Power Supply
	22 uF	X5R 0805	2	1	1	Midway between GPU and Power Supply

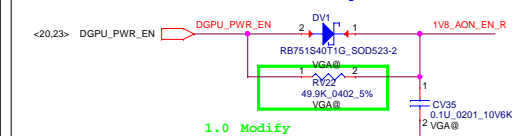


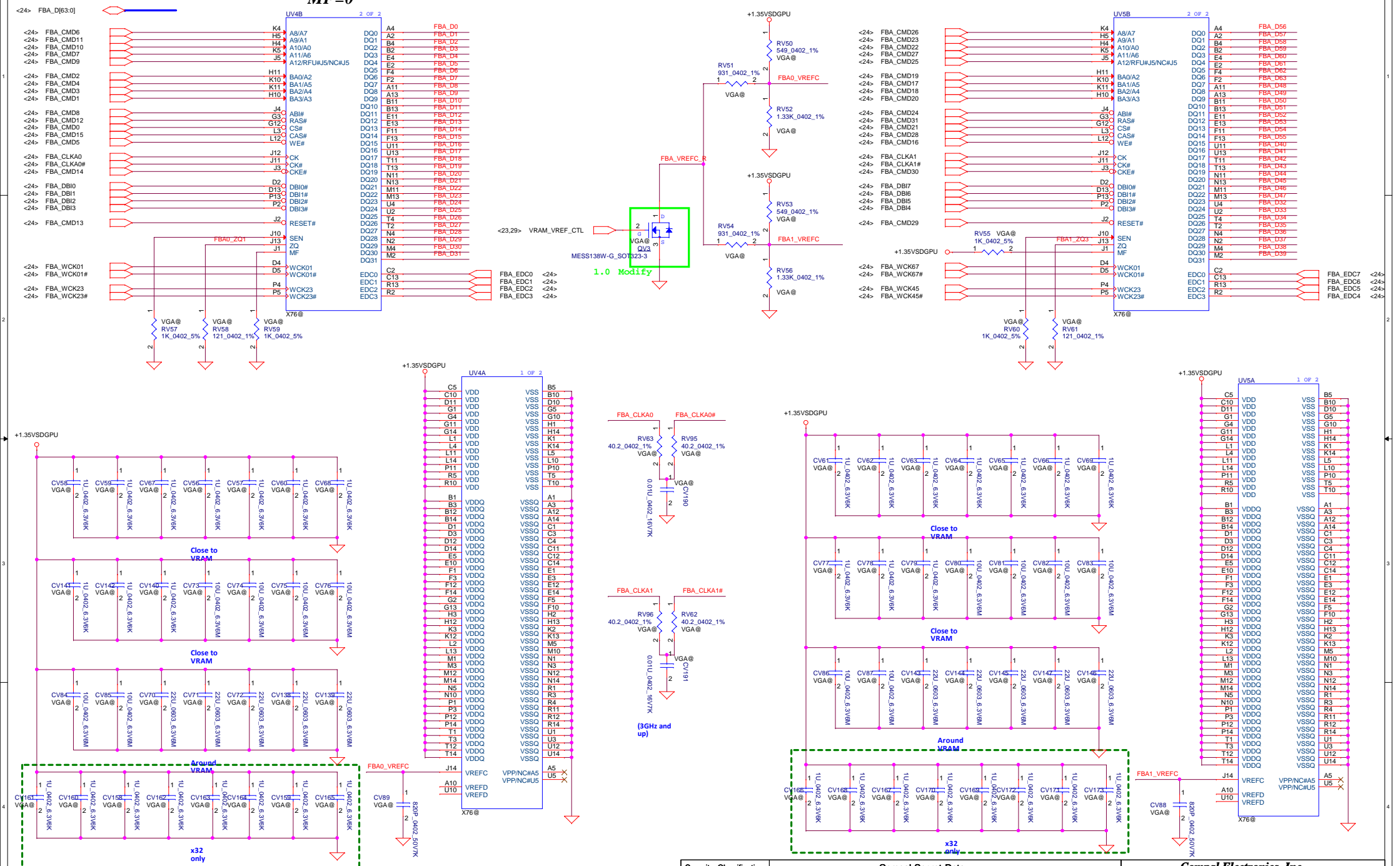
+1.8V_AON/+1.8V_MAIN



WVF		Part 6 of 7	
A2	GND.0	GND.100	D2
17	GND.1	GND.101	D31
18	GND.2	GND.102	D33
20	GND.3	GND.103	E10
22	GND.4	GND.104	E22
114	GND.5	GND.105	E25
116	GND.6	GND.106	E5
118	GND.7	GND.107	E6
119	GND.8	GND.108	F28
82	GND.9	GND.109	F7
21	GND.10	GND.110	G10
23	GND.11	GND.111	G13
28	GND.12	GND.112	G16
30	GND.13	GND.113	G19
32	GND.14	GND.114	G2
33	GND.15	GND.115	G22
85	GND.16	GND.116	G25
87	GND.17	GND.117	G28
113	GND.18	GND.118	G3
115	GND.19	GND.119	G30
117	GND.20	GND.120	G32
118	GND.21	GND.121	G33
113	GND.22	GND.122	G5
20	GND.23	GND.123	G7
22	GND.24	GND.124	G6
24	GND.25	GND.125	K28
28	GND.26	GND.126	K30
30	GND.27	GND.127	K32
32	GND.28	GND.128	K5
33	GND.29	GND.129	K7
85	GND.30	GND.130	M13
87	GND.31	GND.131	M15
110	GND.32	GND.132	M17
113	GND.33	GND.133	M18
116	GND.34	GND.134	M20
118	GND.35	GND.135	M22
119	GND.36	GND.136	M2
122	GND.37	GND.137	N14
124	GND.38	GND.138	N12
28	GND.39	GND.139	N16
29	GND.40	GND.140	N19
30	GND.41	GND.140	N2
32	GND.42	GND.141	N21
33	GND.43	GND.142	N23
85	GND.44	GND.143	N28
87	GND.45	GND.144	N30
110	GND.46	GND.145	N33
113	GND.47	GND.146	N33
116	GND.48	GND.147	N5
118	GND.49	GND.148	N7
119	GND.50	GND.149	P13
12	GND.51	GND.150	P15
14	GND.52	GND.151	P17
15	GND.53	GND.152	P18
18	GND.54	GND.153	P20
20	GND.55	GND.154	P22
21	GND.56	GND.155	R12
22	GND.57	GND.156	R14
24	GND.58	GND.157	R16
26	GND.59	GND.158	R19
28	GND.60	GND.159	R21
30	GND.61	GND.160	R23
32	GND.62	GND.161	T13
33	GND.63	GND.162	T15
85	GND.64	GND.163	T18
87	GND.65	GND.164	T17
110	GND.66	GND.165	T2
113	GND.67	GND.166	T20
116	GND.68	GND.167	T22
118	GND.69	GND.168	AG11
119	GND.70	GND.169	F28
12	GND.71	GND.170	T32
13	GND.72	GND.171	T5
16	GND.73	GND.172	T7
17	GND.74	GND.173	U12
22	GND.75	GND.174	U14
25	GND.76	GND.175	U16
30	GND.77	GND.176	U19
34	GND.78	GND.177	U21
37	GND.79	GND.178	U23
81	GND.80	GND.179	V12
82	GND.81	GND.180	V16
83	GND.82	GND.181	V19
84	GND.83	GND.182	V21
85	GND.84	GND.183	V23
86	GND.85	GND.184	W13
87	GND.86	GND.185	W15
88	GND.87	GND.186	W17
89	GND.88	GND.187	W18
90	GND.89	GND.188	W20
91	GND.90	GND.189	W22
92	GND.91	GND.190	W28
93	GND.92	GND.191	X12
94	GND.93	GND.192	X14
95	GND.94	GND.193	Y16
96	GND.95	GND.194	Y19
97	GND.96	GND.195	Y21
98	GND.97	GND.196	Y23
99	GND.98	GND.197	ZH11
07	GND.99	GND.198	ZH11
		GND.199	C16
		GND.200	W32

For Power down sequence



$$MF=1$$
$$MF=0$$


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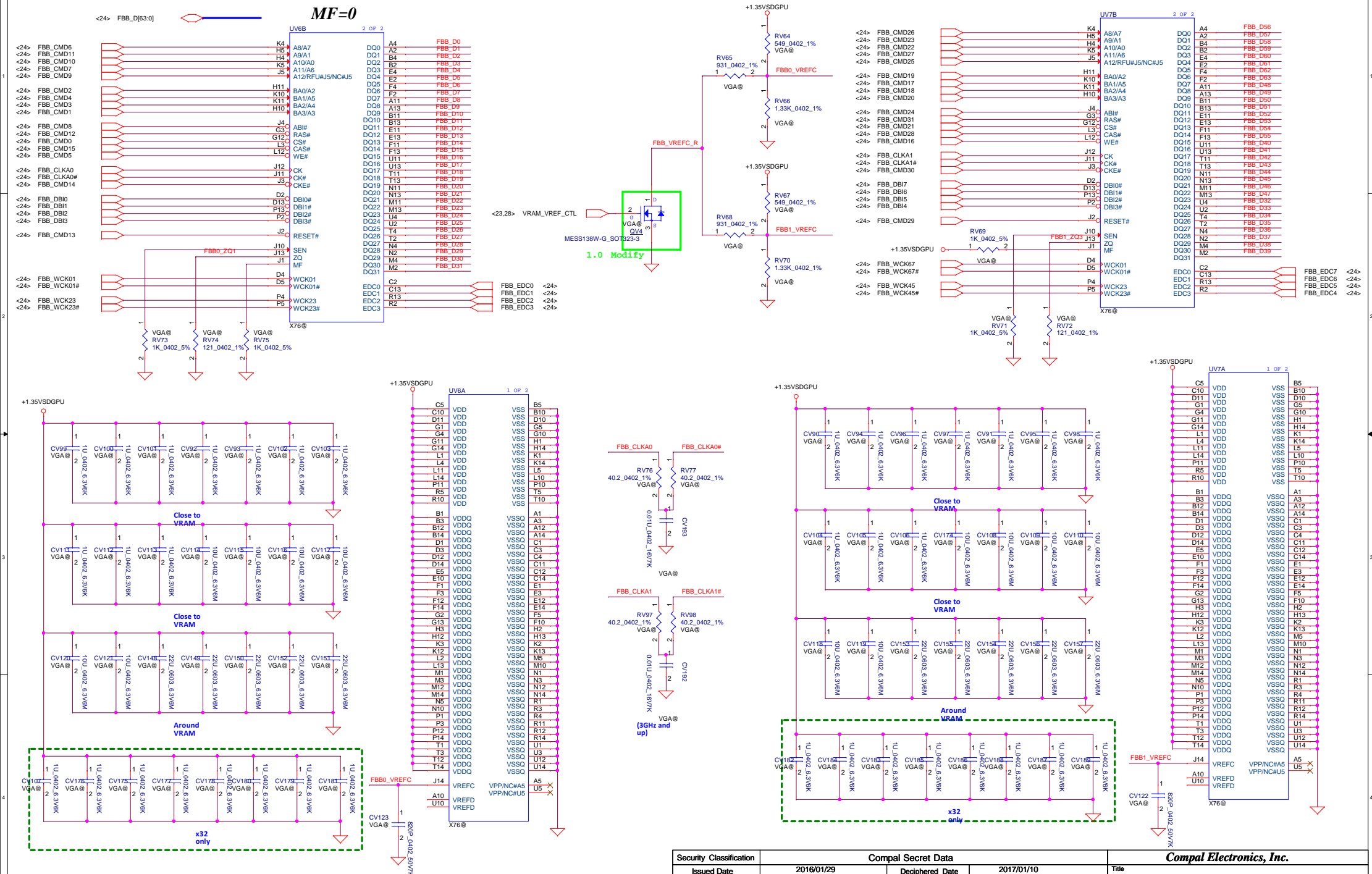
M/P LA E011P

Tuesday, April 11, 2017 Sheet 29 of 64

Friday, April 11, 2017

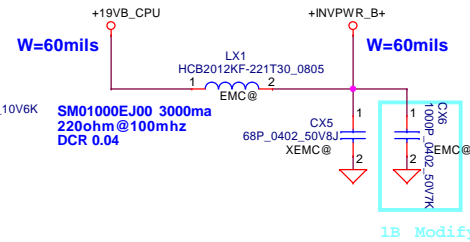
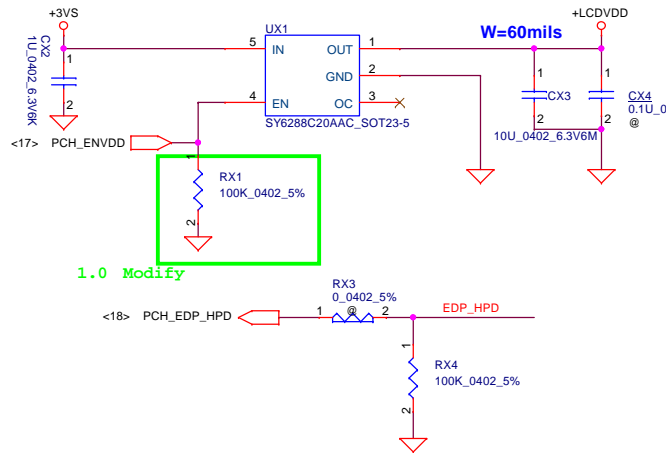
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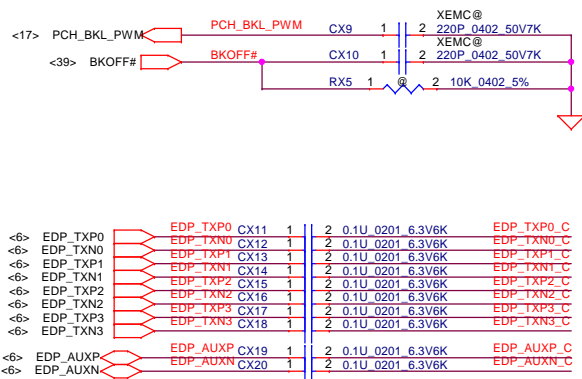
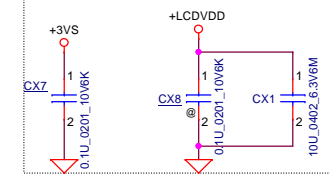


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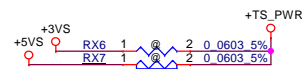
LCD POWER CIRCUIT



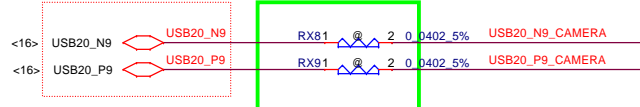
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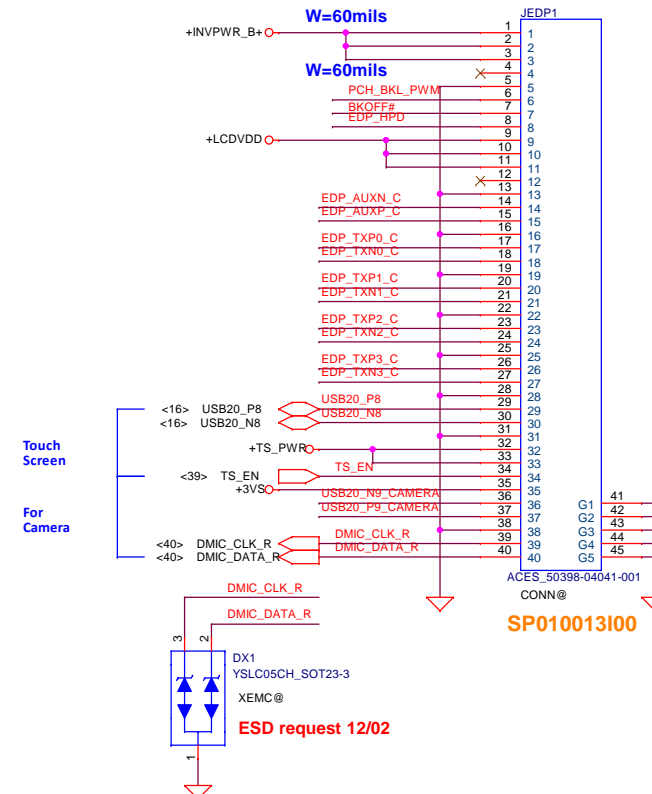
Touch Screen



Camera

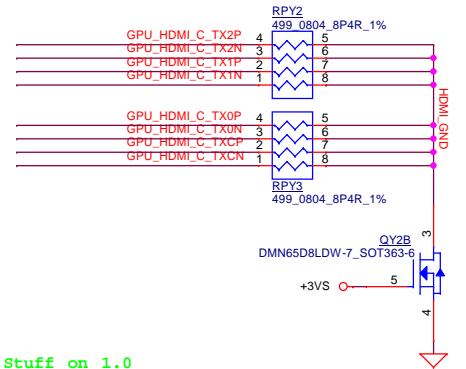
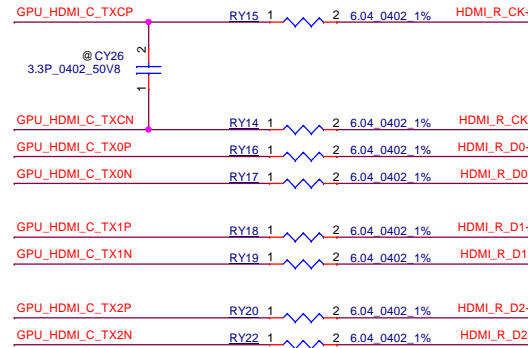
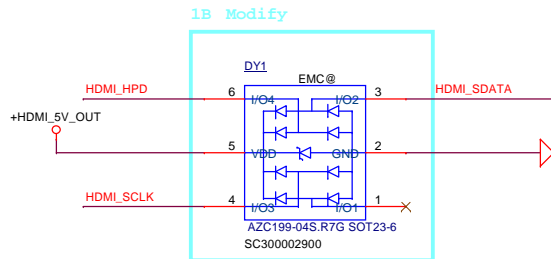
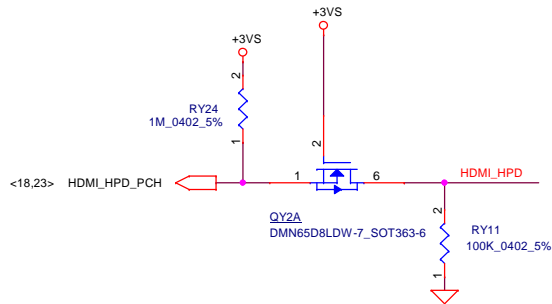
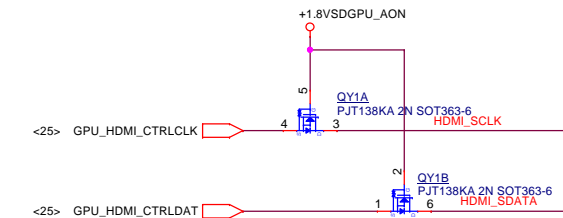


LED PANEL Conn.

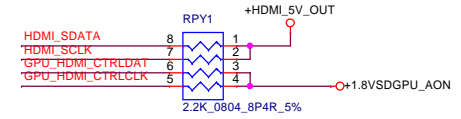
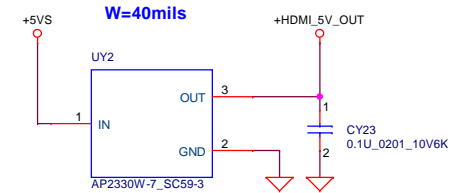
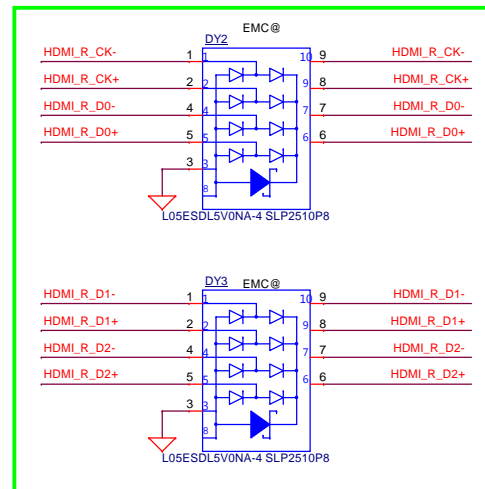


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2017/01/10				Title				eDP CONN.			
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Custom				Document Number				1A			
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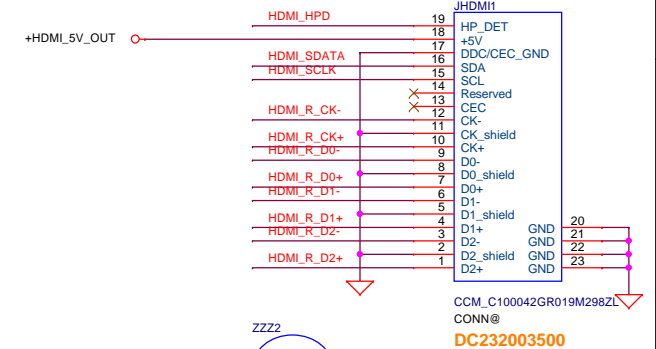
<25>	GPU_HDMI_TXCP	CY22	1	2	.1U_0402_16V7K	GPU_HDMI_C_TXCP
<25>	GPU_HDMI_TXCN	CY24	1	2	.1U_0402_16V7K	GPU_HDMI_C_TXCN
<25>	GPU_HDMI_TX0P	CY16	1	2	.1U_0402_16V7K	GPU_HDMI_C_TX0P
<25>	GPU_HDMI_TX0N	CY17	1	2	.1U_0402_16V7K	GPU_HDMI_C_TX0N
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<25>	GPU_HDMI_TX1N	CY19	1	2	.1U_0402_16V7K	GPU_HDMI_C_TX1N
<25>	GPU_HDMI_TX2P	CY20	1	2	.1U_0402_16V7K	GPU_HDMI_C_TX2P
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Stuff on 1.0

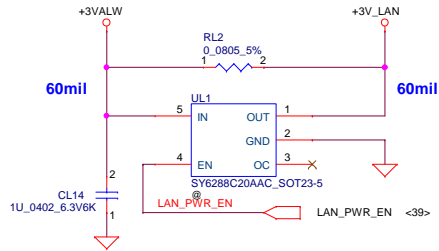


HDMI connector

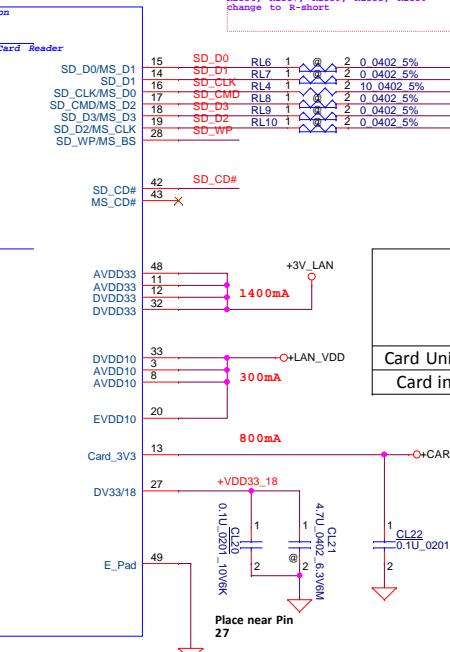
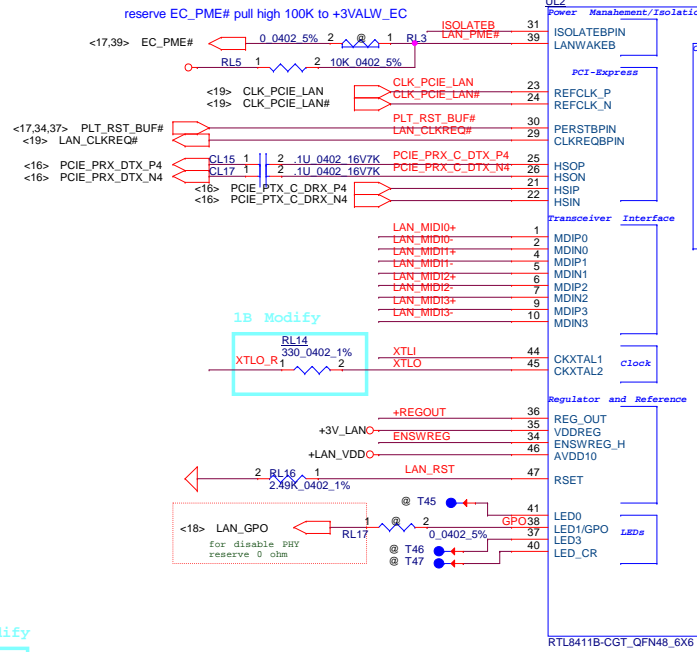
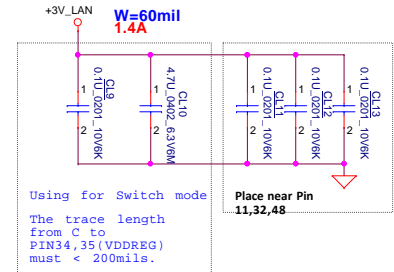
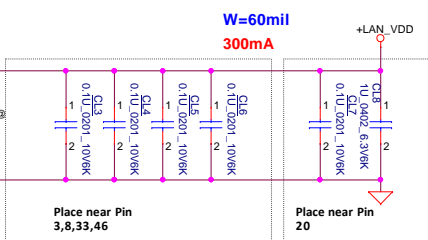
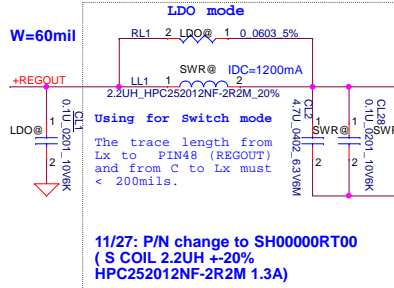


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Date				Tuesday, April 11, 2017				Document Number			
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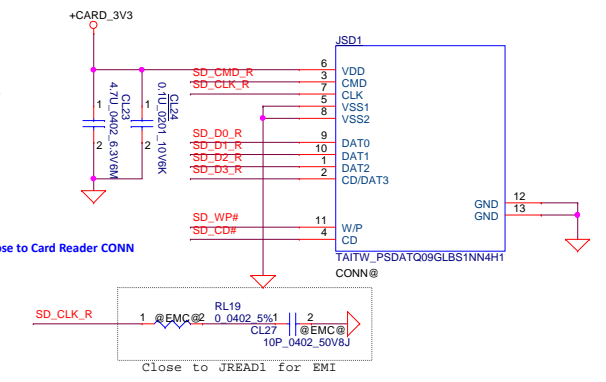
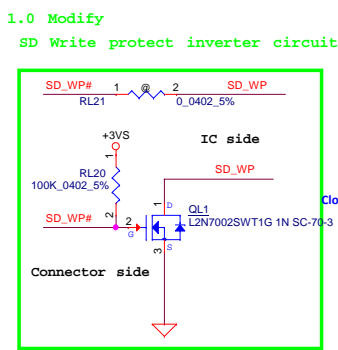
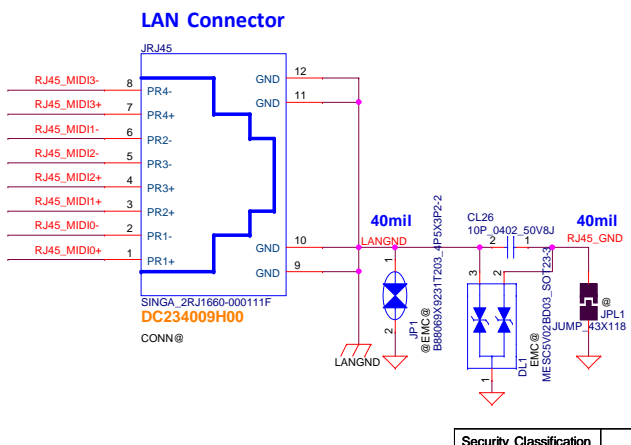
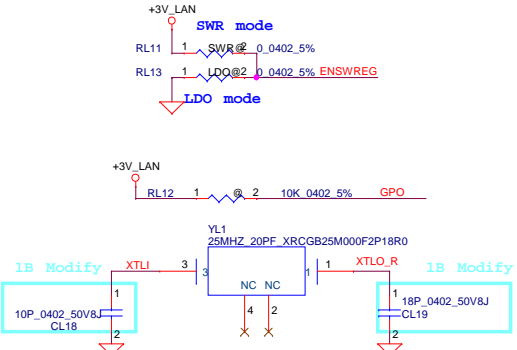
LAN-RTL8411B



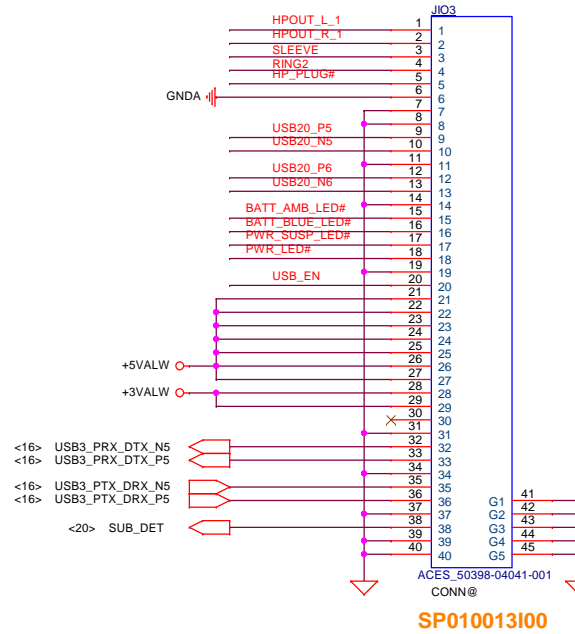
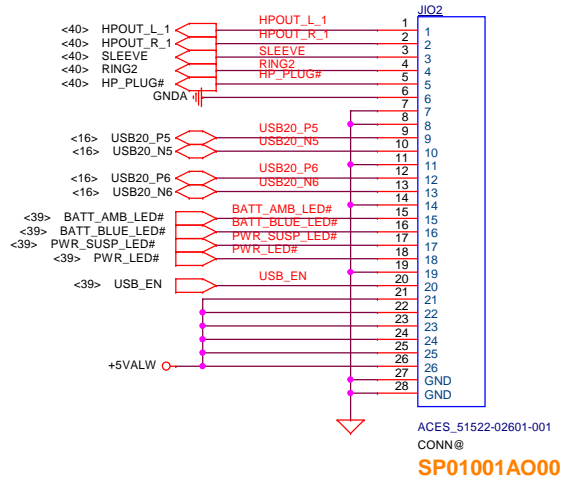
From EC
High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5-2.8A
+3V_LAN Rising time must >0.5ms and <100ms



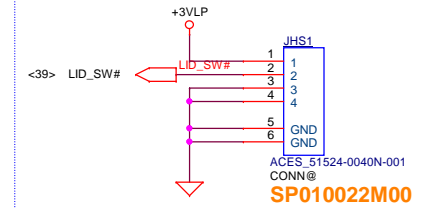
	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close



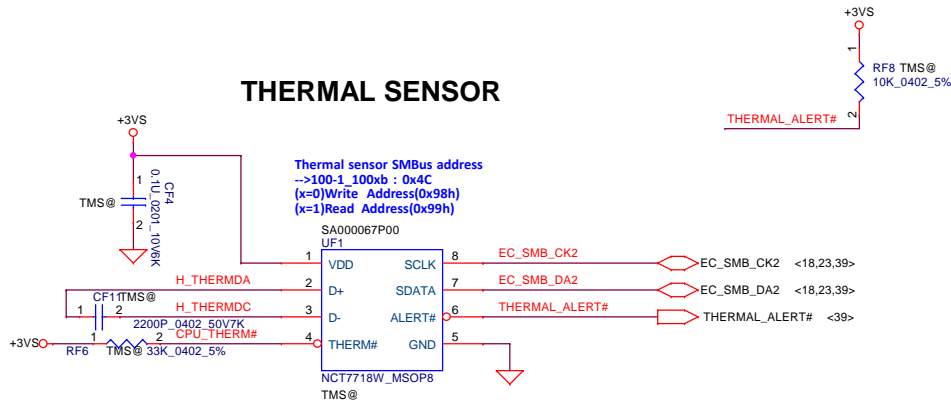
To USB/B Co lay CONN



To Hall sensor/B

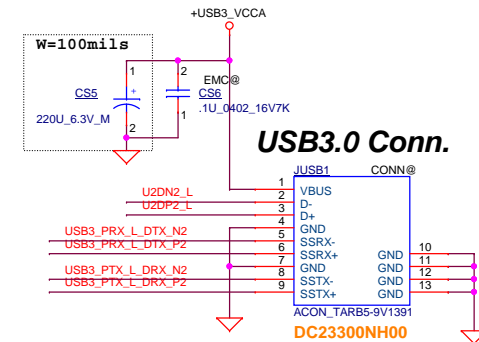
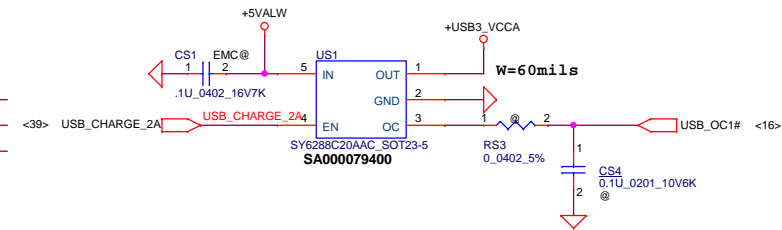
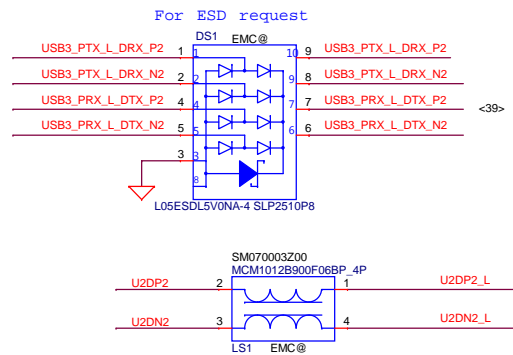
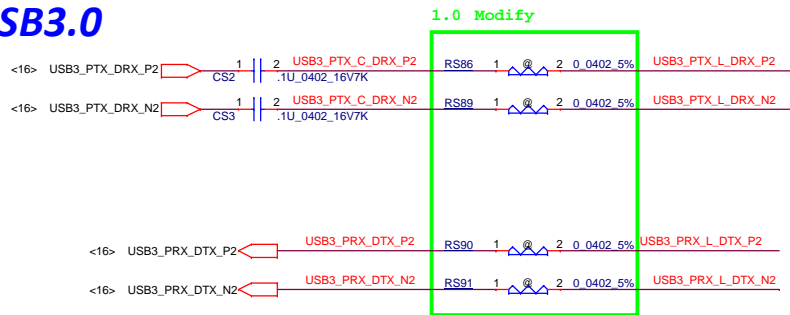


THERMAL SENSOR



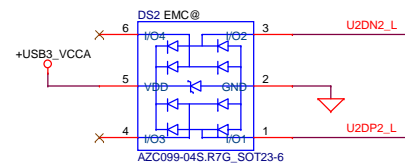
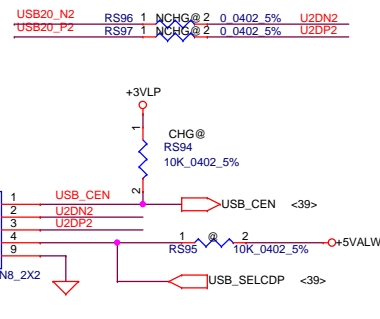
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Issued Date	2016/11/03	Deciphered Date	2017/01/10	Title	FUN/B & LED/B
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USB3.0



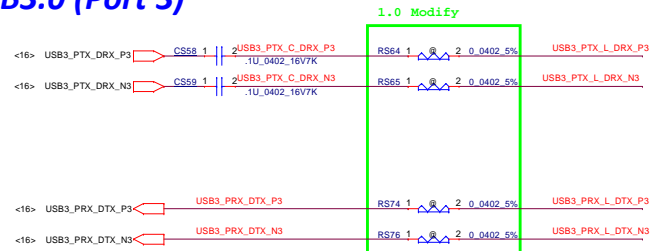
USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only

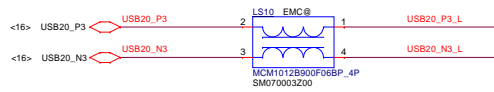
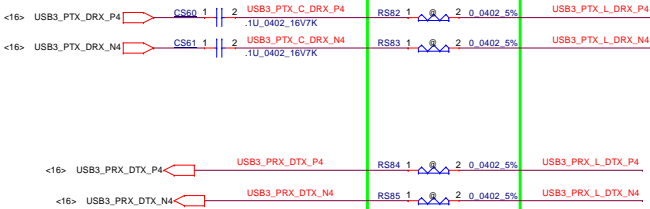


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USB3.0 (Port 3)



USB3.0 (Port 4)



For ESD request

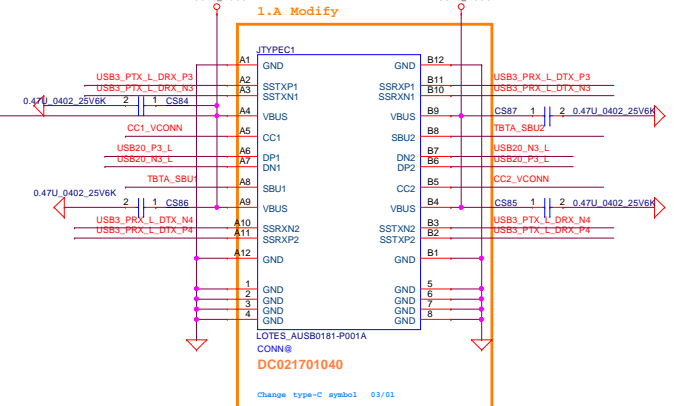
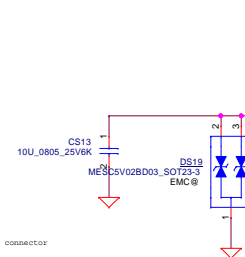
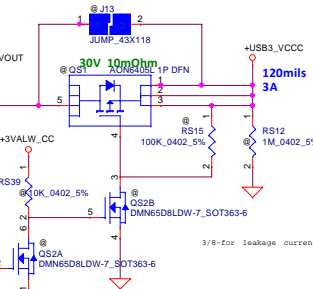
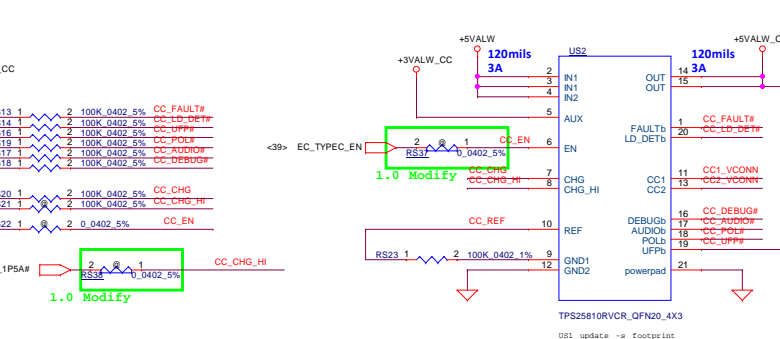
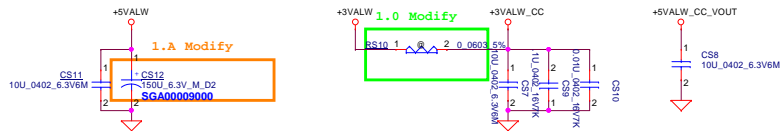
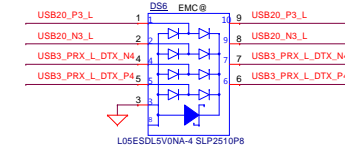
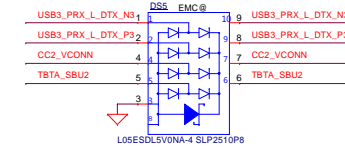
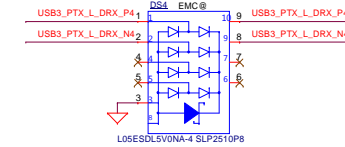
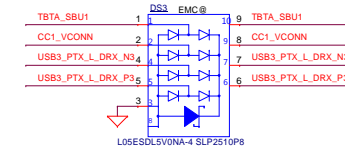


Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

EC_TYPEC_EN	S0	S3	S5
AC Mode (Adapter In)	On	On	Off
DC Mode (Battery Only)	On	On	Off

Note 1: Stop charge current when the battery capacity is below a specified percentage.

Note : 2017 BIOS SPEC define DC mode 30% stop charge

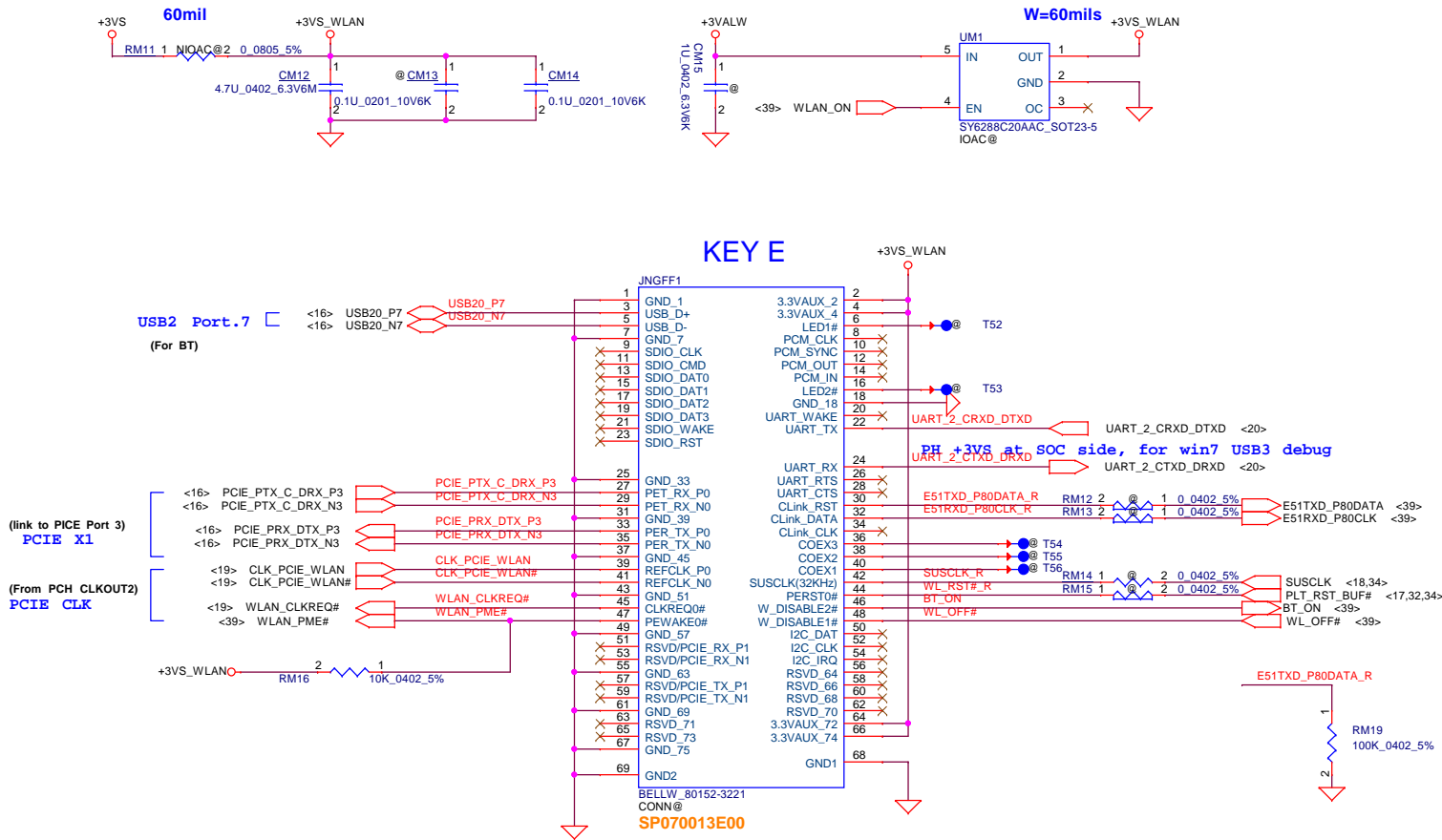
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Compal Electronics, Inc.

CC+USB TYPE C

CSMMH M/B LA-E911P

Wireless LAN

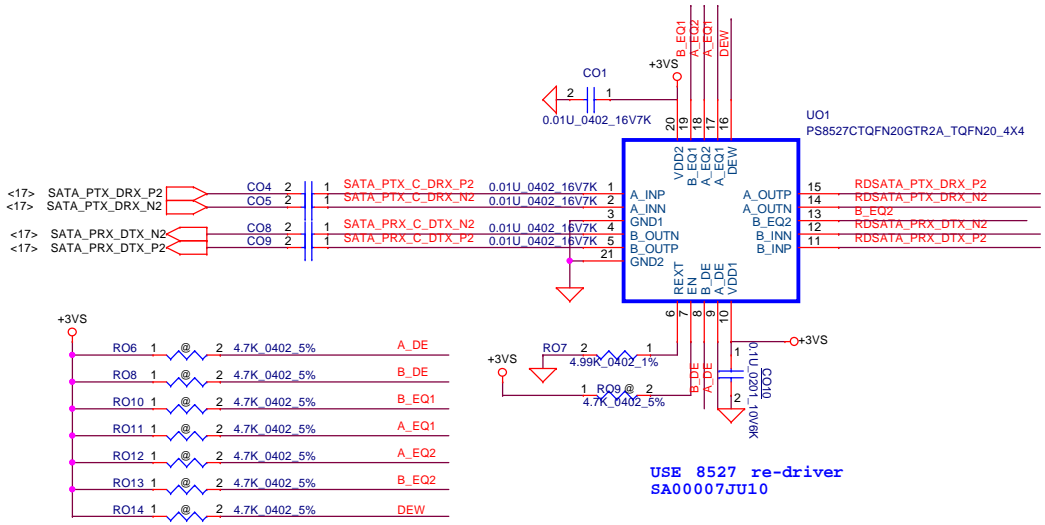


NGFF WL+BT (KEY E)

74	SDP	GND	75
72	SDP	RESERVED/REFCLKN1	73
70	UM_Power_SRC/GPIO2/PEWake1#	RESERVED/REFCLKP1	71
68	UM_Power_SINK/CLKREQ0#	GND	69
66	UM_SWP/PERST1#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (IO/Q3.3)	GND	63
60	DC CLK (IO/Q3.3)	Reserved/PETn1	61
58	DC DATA (IO/Q3.3)	Reserved/PETp1	59
56	W_DISABLE1# (IO/Q3.3V)	GND	57
54	Reserved/W_DISABLE2# (IO/Q3.3V)	PEWake0# (IO/Q3.3V)	55
52	PERST0# (IO/Q3.3V)	CLKREQ0# (IO/Q3.3V)	53
50	SUSCLK(32KHz) (IO/Q3.3V)	GND	51
48	COEX1 (IO/Q1.8V)	REFCLKND	49
46	COEX2# (IO/Q1.8V)	REFCLKPD	47
44	COEX3# (IO/Q1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART1RTS (IO/Q1.8V)	PETn0	37
34	UART1CTS (IO/Q1.8V)	PETp0	35
32	UART1TX (IO/Q1.8V)	GND	33
30	UART1RX (IO/Q1.8V)	SDIO_RESET# (IO/Q1.8V)	29
28	UART2RTS (IO/Q1.8V)	SDIO_WAKE# (IO/Q3.3V)	27
26	UART2CTS (IO/Q1.8V)	SDIO_DATA7# (IO/Q1.8V)	25
24	UART2TX (IO/Q1.8V)	SDIO_DATA7 (IO/Q1.8V)	23
22	UART2RX (IO/Q1.8V)	SDIO_DATA6# (IO/Q1.8V)	21
20	UART2RTS (IO/Q1.8V)	SDIO_DATA6 (IO/Q1.8V)	19
18	UART2CTS (IO/Q1.8V)	SDIO_DATA5# (IO/Q1.8V)	17
16	UART2TX (IO/Q1.8V)	SDIO_DATA5 (IO/Q1.8V)	15
14	UART2RX (IO/Q1.8V)	SDIO_DATA4# (IO/Q1.8V)	13
12	UART2RTS (IO/Q1.8V)	SDIO_DATA4 (IO/Q1.8V)	11
10	UART2CTS (IO/Q1.8V)	SDIO_DATA3# (IO/Q1.8V)	9
8	UART2TX (IO/Q1.8V)	SDIO_DATA3 (IO/Q1.8V)	7
6	UART2RX (IO/Q1.8V)	SDIO_DATA2# (IO/Q1.8V)	5
4	UART2RTS (IO/Q1.8V)	SDIO_DATA2 (IO/Q1.8V)	3
2	UART2CTS (IO/Q1.8V)	SDIO_DATA1# (IO/Q1.8V)	1

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								M.2 Key E (WLAN)			
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SATA Re-Driver and cable HDD Conn.



USE 8527 re-driver
SA00007JU10

Chip Enable, Internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A_DE	De_Empasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

B_DE	De_Empasis
M	-3.5dB(Default)
L	0dB
H	-6dB

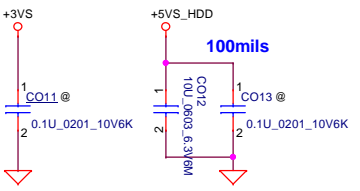
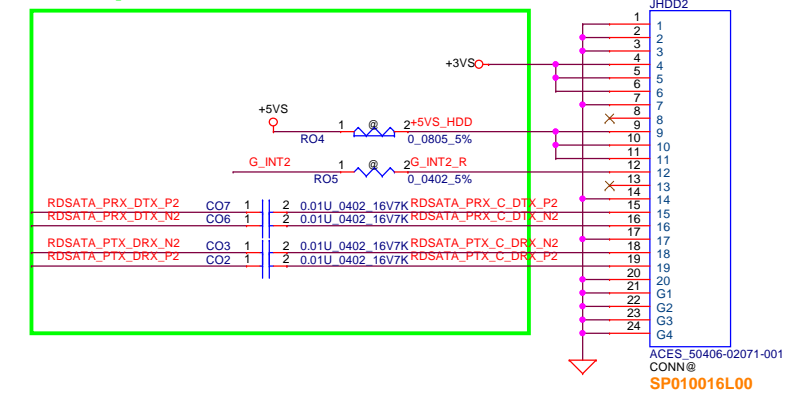
Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

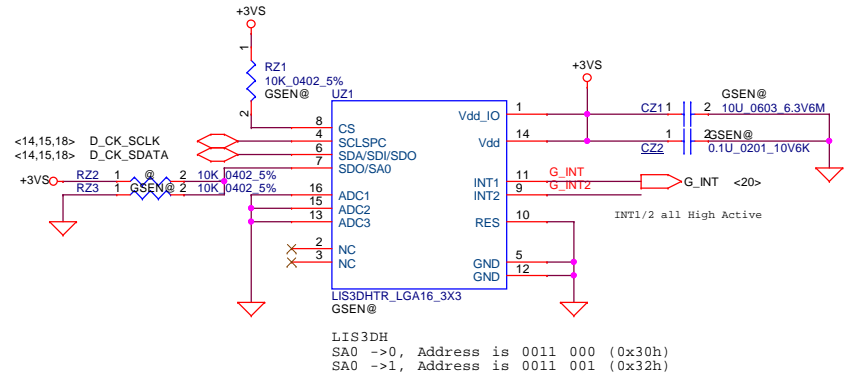
Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

1.0 Modify

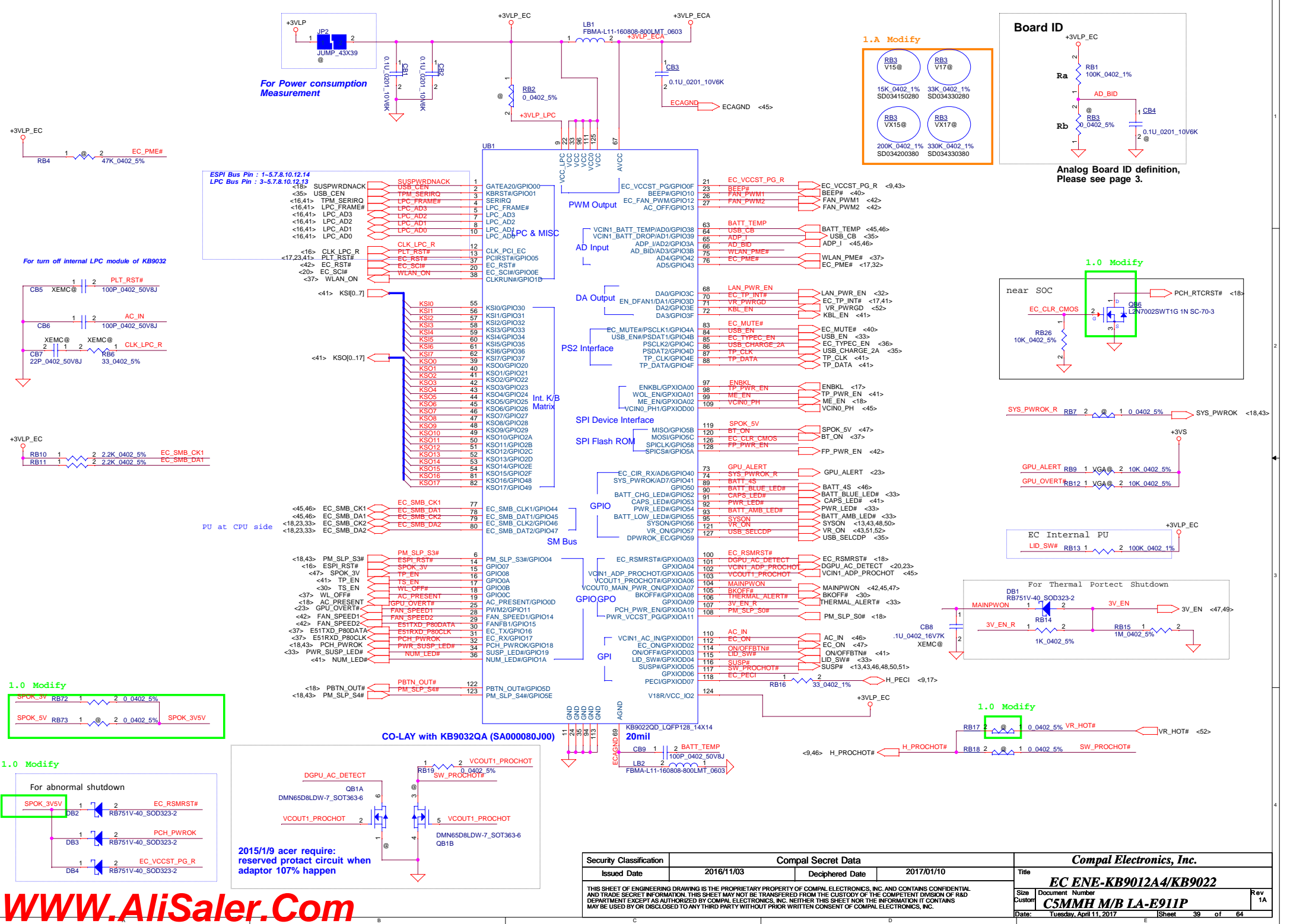


G-Sensor reserved



LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

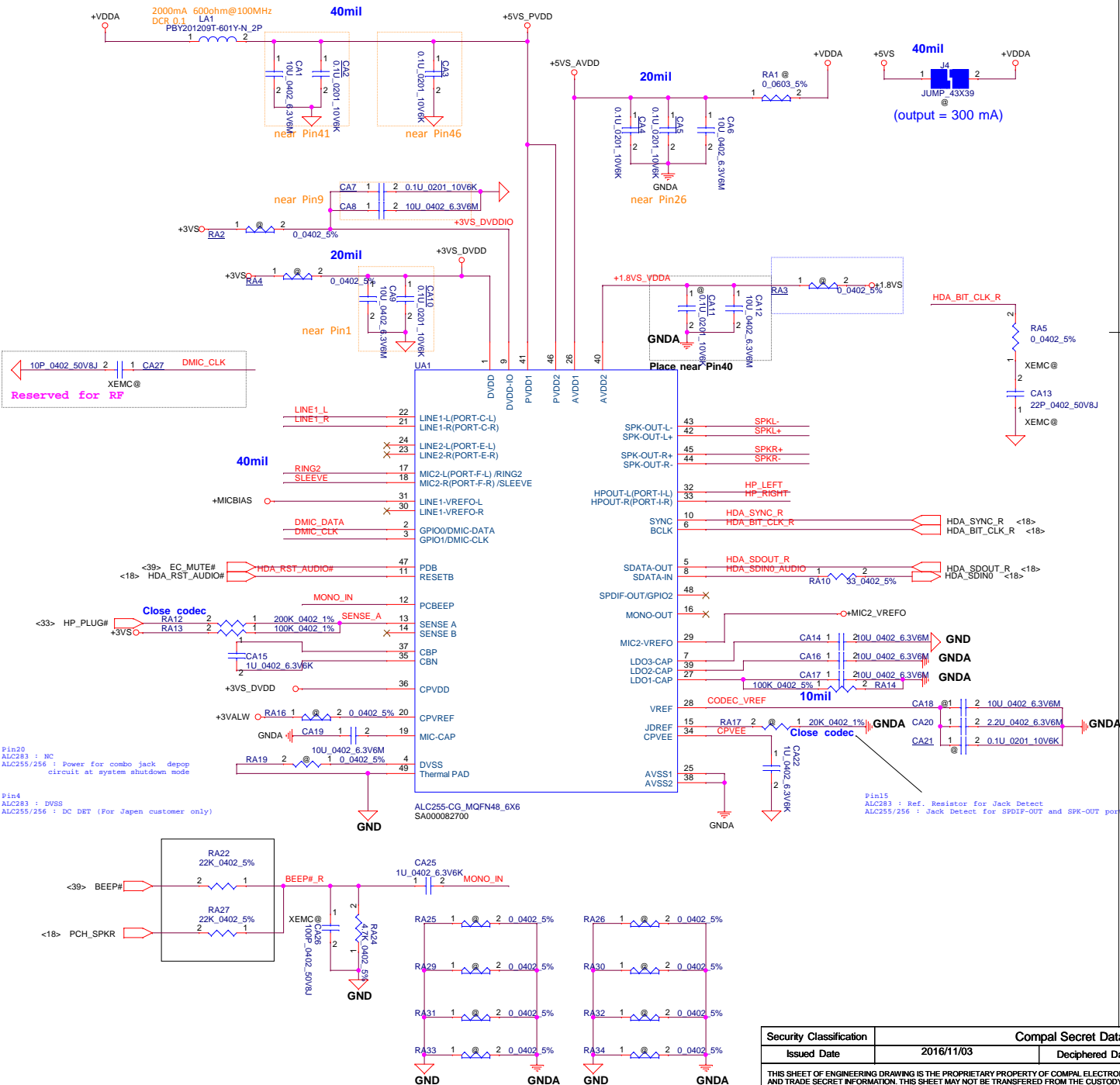
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						Size		Document Number		Rev	
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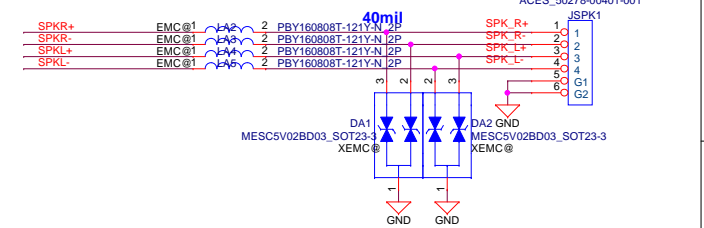
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HD Audio Codec

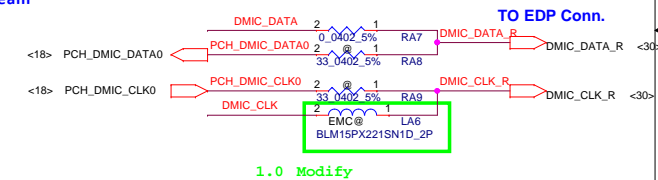


Int. Speaker Conn.



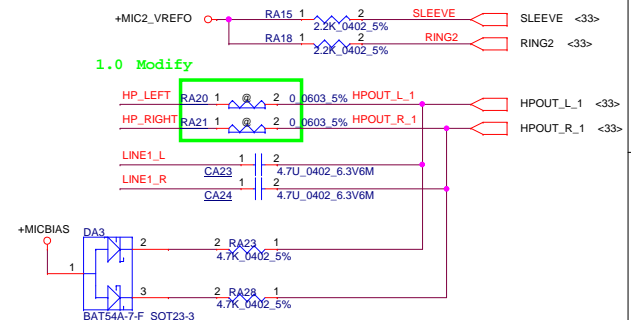
Digital MIC

MIC BOM upload by Audio Team



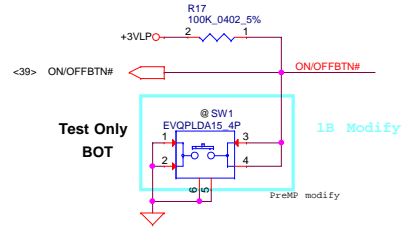
Headphone Out

TO FUN/B

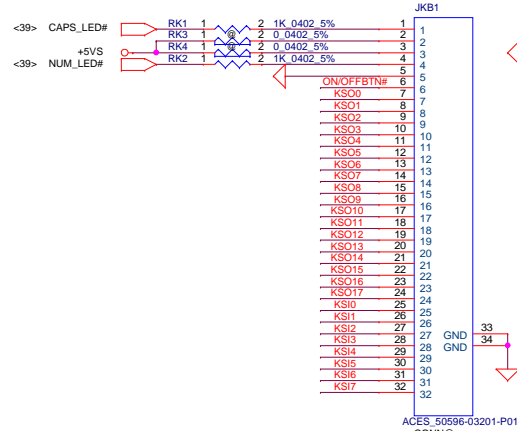


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				Size	Document Number	Rev 1A
				Custm	CSMMH M/B LA-E91IP	
				Date: Tuesday, April 11, 2017		

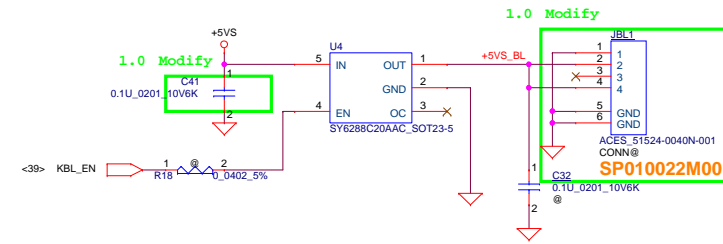
ON/OFF BTN



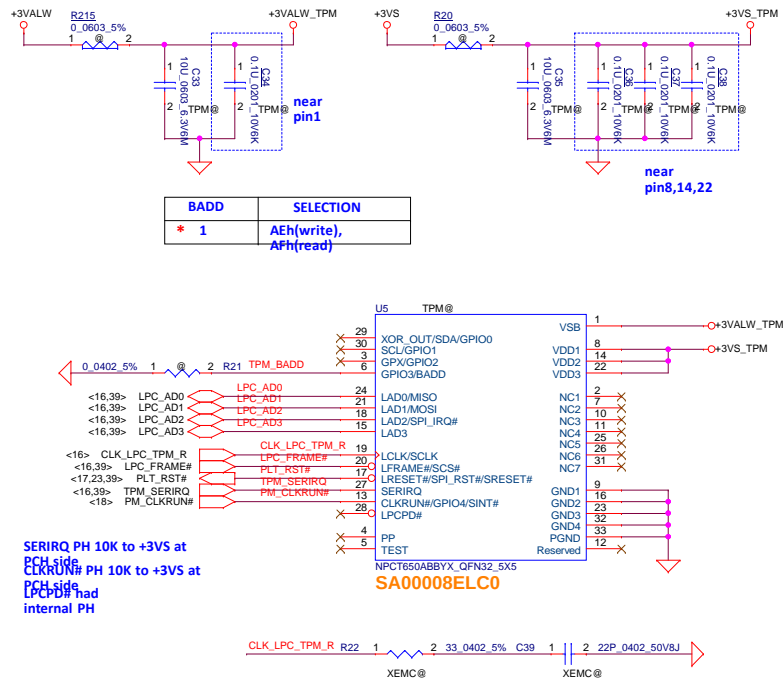
KB Conn.



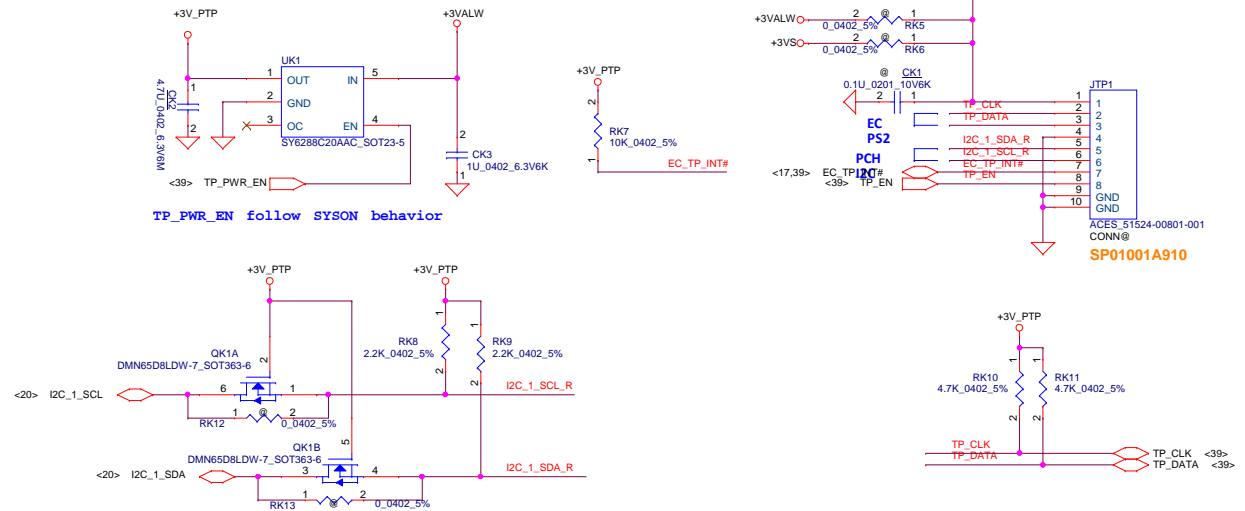
KB BackLight



TPM



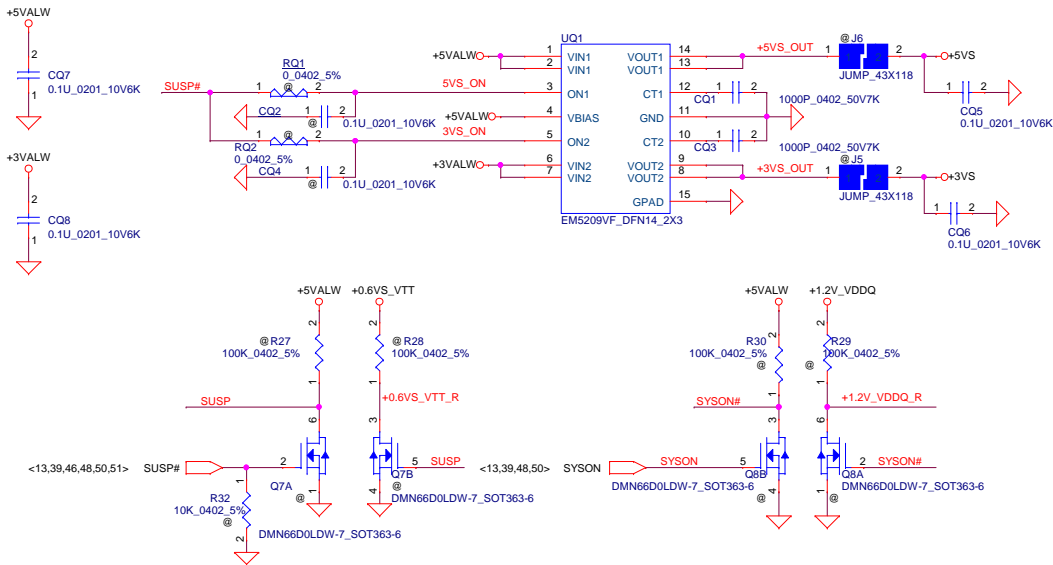
Touch Pad



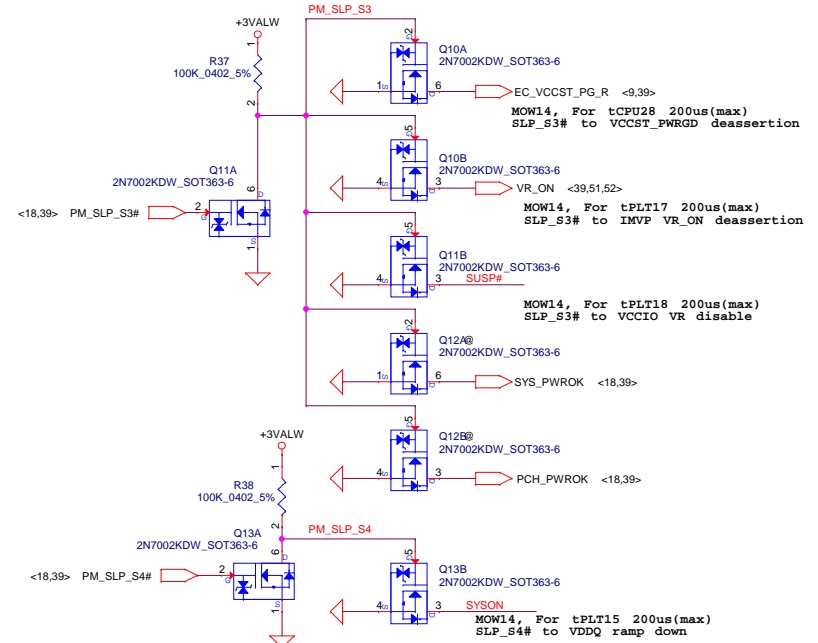
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				Size	Document Number	Rev	
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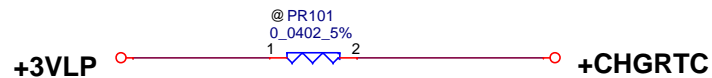
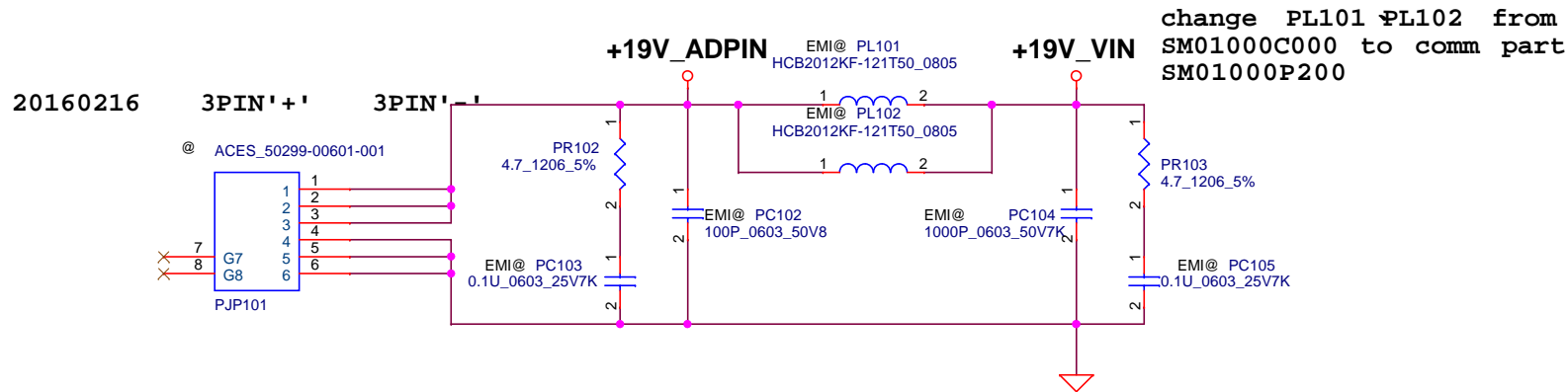
System DC iniferace



For Power ON/Off Sequence



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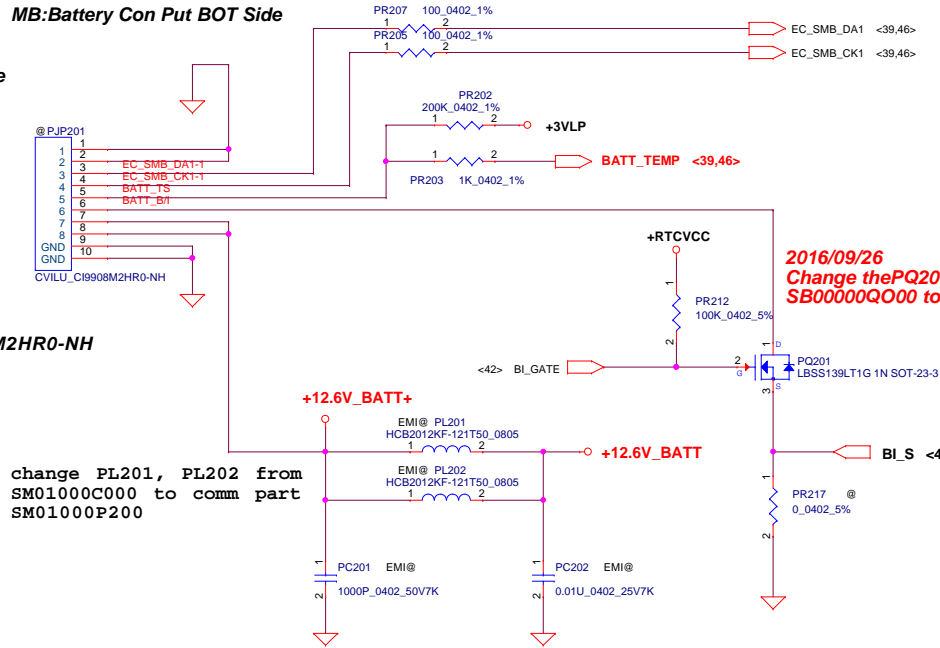
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Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+
PIN9 GND
PIN10 GND
SP020017H00

CVILU_C19908M2HR0-NH

MB:Battery Con Put BOT Side



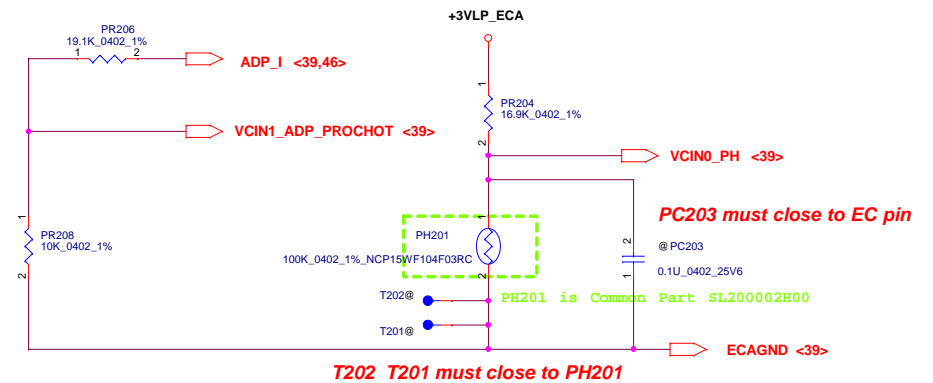
2016/09/26
Change the PQ201 from
SB00000Q000 to SB00001GD00,

2016/08/16 update

For KB9022 sense 20mΩ	Active	Recovery
135W PR206 19.1K ohm SD034191280	175W, 0.63V	175W, 0.63V
135W PR206 19.1K ohm SD034191280	175W, 0.63V	175W, 0.63V

When PR204=16.9K

For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92'C, 1V	56'C, 2V
PH202(ohm)	7.3092K	26.11K



$$ADP_I = 20 * I(\text{adapter}) * 0.01$$

$$I(\text{adapter}) = \text{adapter}(W) * 95\% / 19$$

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+19VB

change PL501 from
SM01000C000 to comm
part SM01000P200

Choke 1uH SH00000YE00 (Common Part)
(Size:6.86 x 6.47 x 3 mm)
(DCR:6.2m~7.2m Ohm)

H/S AON7408 Rds(on) :typ:27m Ohm, max:34m Ohm
Idsm(TA=25)=7.5A, Idsm(TA=70)=5.5A

L/S SI7716 Rds(on) :typ:13.5m Ohm, max:16.5m Ohm
Idsm(TA=25)=16A, Idsm(TA=70)=9.5A

Choke: 7x7x3
Rdc=6.2mohm(Typ), 7.2mohm(Max)

Switching Frequency: 530kHz
Ipeak=7A, Imax=4.9A

VFB=0.607V, Vout=1.214V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

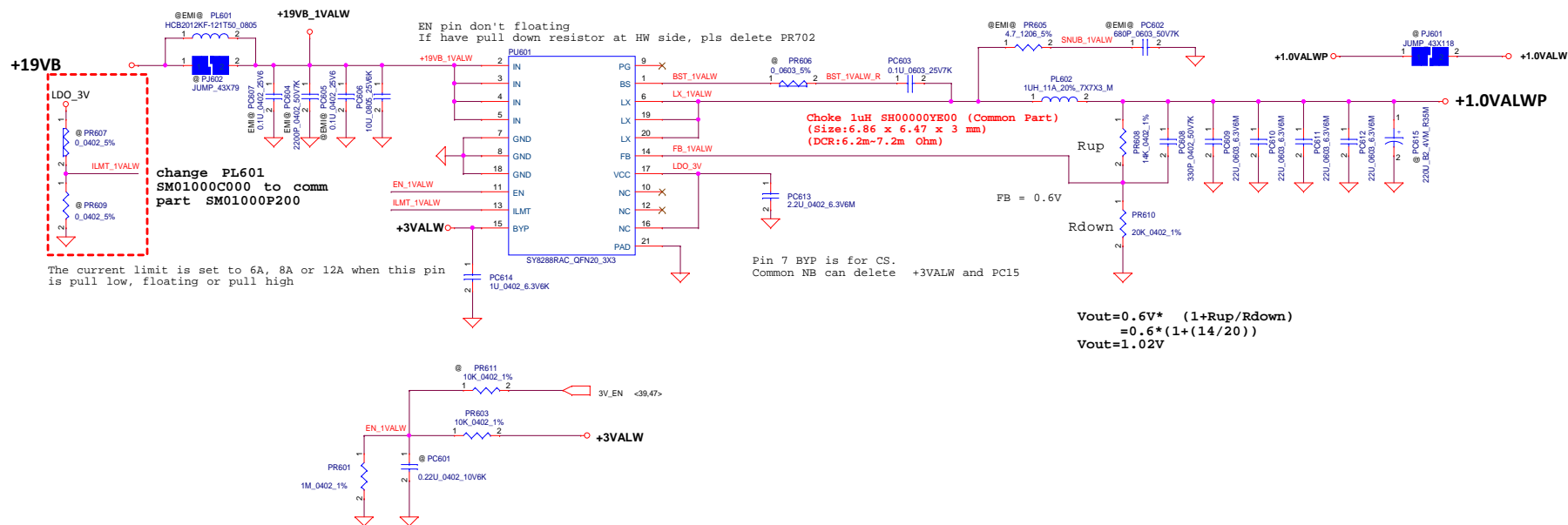
Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A

$$V_{out} = 0.75V * \left(\frac{1 + R_{up}/R_{down}}{1 + (6.19/10)} \right) = 1.214V \quad 1.2\%$$

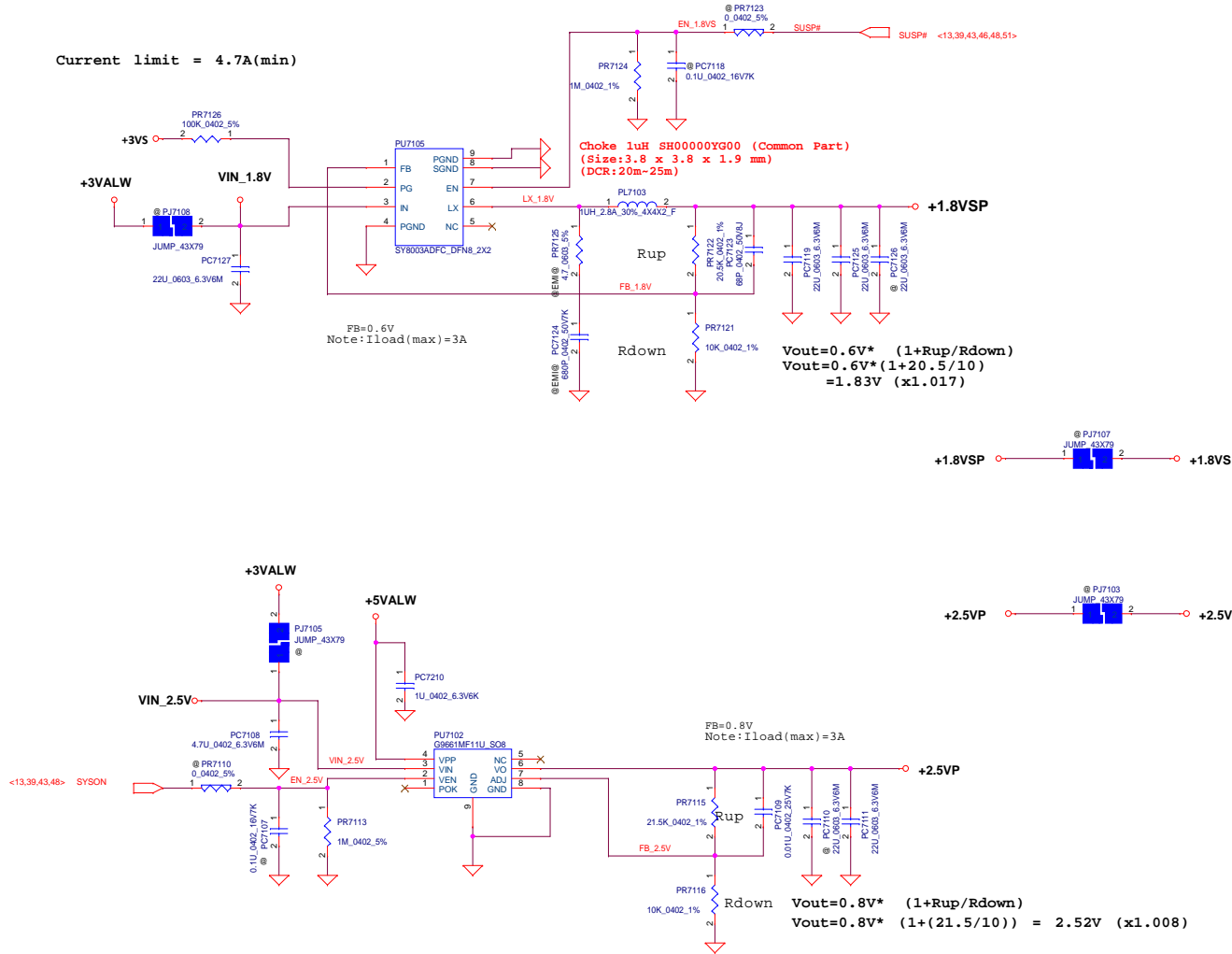
$$V_{out} = 0.75V * \left(\frac{1 + R_{up}/R_{down}}{1 + (8.2/10)} \right) = 1.365V \quad 1.1\%$$

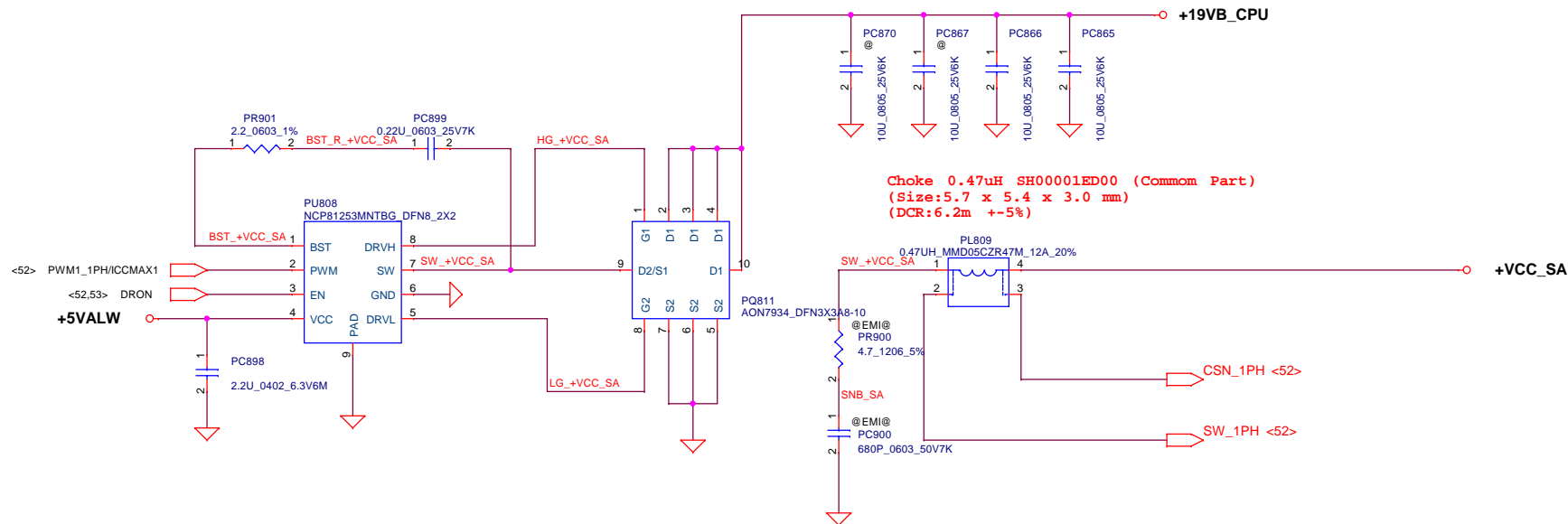
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Current limit = 4.7A(min)





For H-line 42 :
VCC_SA (LL=10m)
FSW = 600kHz
DCR = 6.2m Ohm +/- 5%

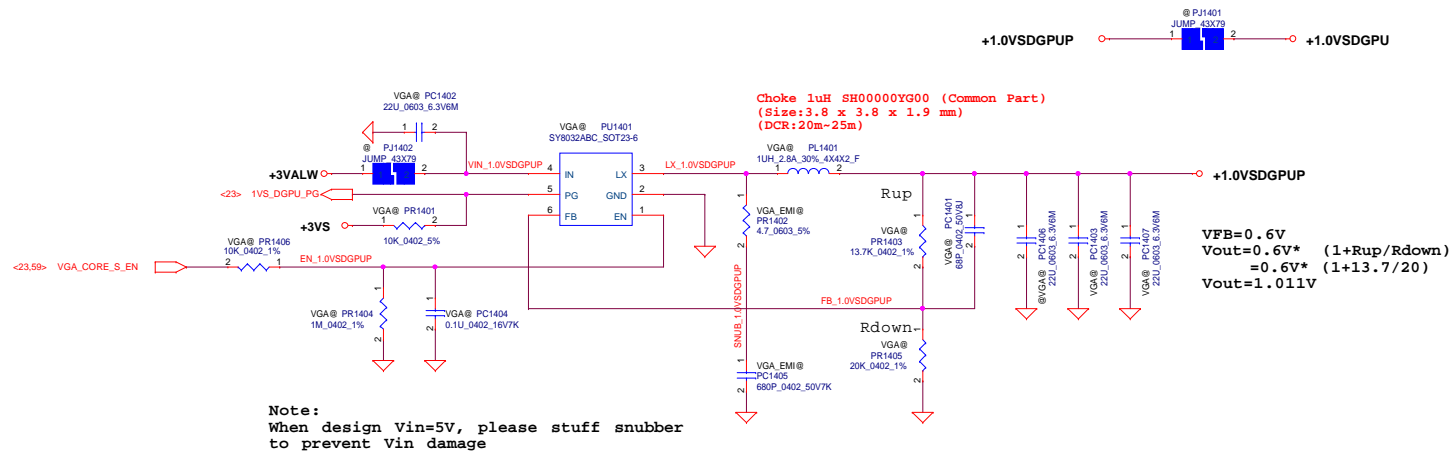
I(max)=10A
I(peak)=12A
Vboot=1.05V

DaulMOS AON7934 TYP MAX
H/S Rds(on) = 12.4m Ohm , 15.8m Ohm
L/S Rds(on) = 9.1m Ohm , 11.6m Ohm

Function Field :
Drivers - 36.2
Rest of support elements - 36.3

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